SIMATIC S5

IP 240
Counter/Positioning/
Position Decoder Module

Manual

EWA 4NEB 811 6120-02b

Edition 03

Only qualified personnel should install or maintain this equipment after becoming thoroughly familiar with all warnings, safety notices, and maintenance procedures contained in this manual. The successful and safe operation of this equipment is dependent upon proper handling, installation, operation, and maintenance.

The following are definitions of the terms “qualified person,” “danger,” “warning,” and “caution,” as applicable for this document.

Qualified Person
One who is familiar with the installation, construction, and operation of this equipment and the hazards involved. In addition, the person should have the following qualifications:

- Be trained and authorized to use and tag circuits and equipment in accordance with established safety practices
- Be trained in the proper care and use of protective equipment in accordance with established safety practices
- Be trained in rendering first aid

DANGER
Indicates loss of life, severe personal injury, or substantial property damage will result if proper precautions are not taken.

WARNING
Indicates loss of life, severe personal injury, or substantial property damage can result if proper precautions are not taken.

CAUTION
Indicates minor personal injury or property damage can result if proper precautions are not taken.

First Printing, March 1991
Printed in the Federal Republic of Germany

Supplement to the IP 240 Manual, Order No. 6ES5 998 0TB22, Edition 3

Use of the IP 240 in the S7-400 programmable controller
This manual has been supplemented by Appendices A, B and C. They include information on how to install S5 modules in an S7-400 programmable controller when using an adapter casing.

Replacement Pages for IP 240 Manual, MLFB 6ES5 998 OTB22, Edition 3

The current manual is valid for the following modules:
- IP 240, MLFB 6ES5 240-1AA21 and
- IP 240, MLFB 6ES5 240-1AA12.

Use with the IP 240, MLFB 6ES5 240-1AA21
The IP 240, MLFB 6ES5 240-1AA21 is a further development of the IP 240, MLFB 6ES5 240-1AA12. With this MLFB, the module was converted to SMD components as far as possible. The changes to the module description required as a result of the changes have been included in Edition 3 of this manual.
The replacement pages at the end of the manual can be ignored in this case.

Use with the IP 240, MLFB 6ES5 240-1AA12
Supplements and changes to the revised module IP 240, MLFB 6ES5 240-1AA21 have been included in Edition 3 of this manual.
To use this manual with the IP 240, MLFB 6ES5 240-1AA12, you must replace the relevant pages of the manual with the following pages 2-1 to 2-8, 3-1 to 3-2, 5-1 to 5-4 and 5-7 to 5-8 (at the end of the manual).
The pages
- for MLFB 6ES5 240-1AA12 have the number 811 6120-01 in the footer
- for MLFB 6ES5 240-1AA21 have the number 811 6120-01a in the footer

Preface

In addition to open and closed-loop control, the programmable controllers of the SIMATIC S5 family execute special tasks such as positioning and counting. So that these auxiliary functions do not unnecessarily load the central processor (S5 CPU), they are handled by standalone "intelligent" I/O modules. These have their own microprocessors and execute special time-critical tasks autonomously.

The two-channel IP 240 module is suitable for the following applications:

- **Position decoding**
  The IP 240 counts and processes pulses from incremental encoders. Cam controllers and limit switches can be simulated by comparing the actual value with preset tracks.
- **Counting**
  The IP 240 is suitable for gate-controlled counting of rapid pulse trains and for initiating specific reactions when the count reaches zero.
- **IP 252 expansion**
  The IP 240 operates as a slave for the IP 252 closed-loop control module, thus allowing the connection of other incremental encoders to the IP 252. The acquired signals are transferred direct to the IP 252.
- **Positioning**
  The IP 240 enables controlled positioning with cutoff points. As many as 254 positions can be stored on the IP for this purpose. When a position has been selected, either the direction of travel or the traversing speed can be specified directly over the IP outputs. The approach is controlled and monitored via three selectable operating distance ranges. Incremental encoders are used for position sensing.

The module can intervene direct in the process or flag process states over four digital outputs (two per channel).

The IP 240 has interrupt capability, making it possible to report certain events direct to the S5 CPU.

Standard software function blocks are available for handling the data interchange between the S5 CPU and the IP 240.

Introduction

The following pages contain information which will help you to use this manual.

Description of Contents

The contents of this manual can be divided into blocks according to topic:

- Module description
- Addressing
- Hardware installation and notes on operation
- Functional description
- Position decoding, counting, IP 252 expansion, positioning
- Direct data interchange with the IP 240
- Response times, encoder signals
- Error messages

At the end of the book you will find correction forms. Please enter any suggestions you may have in the way of improvements or corrections in this form and send it to us. Your comments will help us to improve the next edition.

Courses

SIEMENS provide SIMATIC S5 users with extensive opportunities for training.

For more information, please contact your SIEMENS representative.

Reference Literature

This manual is a comprehensive description of the IP 240. Topics not specific to the IP 240, however, are only briefly dealt with. You will find more detailed information in the following literature:

- **Speicherprogrammierbare Steuerungen SPS** (available in German only)
  Volume 1: Logic and sequential controls; from the control problem to the control program.

  Günter Wellenreuther, Dieter Zastrow
  Braunschweig 1987

  Contents:
  - How a programmable controller works
  - The theory of logic control using the STEP 5 programming language for SIMATIC S5 programmable controllers.

  Order No.: ISBN 3-528-04464-0

- **Automating with the S5-115U**
  SIMATIC S5 programmable controllers

  Hans Berger
  Siemens AG, Berlin and Munich 1989

  Contents:
  - STEP 5 programming language
  - Program processing
  - Integral blocks
  - Interfaces to the peripherals

  Order No.: ISBN 3-8009-1526-X

- **Automating with the S5-135U**
  SIMATIC S5 programmable controllers

  Hans Berger
  Siemens AG, Berlin and Munich 1989

  Contents:
  - STEP 5 programming language
  - Program processing
  - Integral blocks
  - Interfaces to the peripherals
  - Multiprocessor operation

  Order No.: ISBN 3-8009-1537-5

- **Automating with the SIMATIC S5-155U**
  SIMATIC S5 programmable controllers

  Hans Berger
  Siemens AG, Berlin and Munich 1989

  Order No.: ISBN 3-8009-1538-3

You can find information on the range of units in the following catalogs:

- ST 52.3 ”S5-115U Programmable Controller”
- ST 57 ”Standard Function Blocks and Drivers for U-Range Programmable Controllers”
- ST 59 ”S5 Programmers”
- ET 1.1 ”ES 902 C Modular Packaging System 19 in. Design”
- MP 11 Thermocouples, Compensating Boxes

There are separate manuals for other components and modules (e.g. CPUs and SINEC L1). We refer to these information sources at the appropriate points in the text.

Conventions

In order to improve the readability of the manual, a menu-style breakdown was used, i.e.:

- The individual chapters can be quickly located by means of a thumb register.
- There is an overview containing the headings of the individual chapters at the beginning of the manual.
- Each chapter is preceded by a breakdown of its subject matter.
  The individual chapters are subdivided into sections and subsections. Bold face type is used for further subdivisions.
- Pages, figures and tables are numbered separately in each chapter. The page following the chapter breakdown contains a list of the figures and tables appearing in that particular chapter.

Certain conventions were observed when writing the manual. These are explained below.

- A number of abbreviations have been used.
  Example: Central processing unit (CPU)
- Footnotes are identified by a superscript consisting of a small digit (e.g. ”1”) or ”*”. The actual footnote is generally at the bottom of the page or underneath a table.
- Cross-references are shown as follows:
  ”(Section 7.3.2)” refers to subsection 7.3.2.
  No references are made to individual pages.
- Actions required from the user are introduced by the symbol .
- All dimensions in drawings etc. are given in millimetres (mm). This is followed by the value in inches in parentheses. Example: 187 (7.29).
- Values can be expressed by binary, decimal or hexadecimal numbers. The number system is indicated by a subscript; example: $F000_H$.
- Especially important imformation is written in text boxes. A heading in the upper part of the text box defines the meaning of the note.

Note

is important imformation on the product, the handling of the product or parts of documentation that have to be observed very carefully.

Warning

means that loss of life, severe personal injury or substantial property damage can result if proper precautions are not taken.

Manuals can only describe the current version of the programmable controller. Should modifications or supplements become necessary in the course of time, a supplement will be prepared and included in the manual the next time it is revised. The relevant version or edition of the manual appears on the cover. In the event of a revision, the edition number will be incremented by ”1”.

Conventions

The following conventions are used in this book and are listed for your reference:

Convention	Definition	Example
	A box that indicates a type of hazard, describes its implications, and tells you how to avoid the hazard is a cautionary statement. Some cautionary statements include a graphic symbol representing an electrical or radio-frequency hazard. All cautionary statements have one of the following levels of caution: • A danger indicates that loss of life, severe personal injury, or substantial property damage will result if proper precautions are not taken. • A warning indicates that loss of life, severe personal injury, or substantial property damage can result if proper precautions are not taken. • A caution indicates that minor personal injury or property damage can result if proper precautions are not taken.	

Figures

1 System Overview

Intelligent input/output modules (I/Os) extend the field of applications of the SIMATIC S5 programmable controller system. They are technology-oriented and off-load the central processor by preprocessing the input signals.

Digital input modules can resolve pulses up to a frequency of 100 Hz. The IP 240 can be used for applications with higher frequencies and for connecting incremental encoders.

The module can be used in four modes:
- Position decoding
- Counting
- IP 252 expansion (only in the S5-115U programmable controller)
- Positioning

It is configured in the desired mode by the user program.

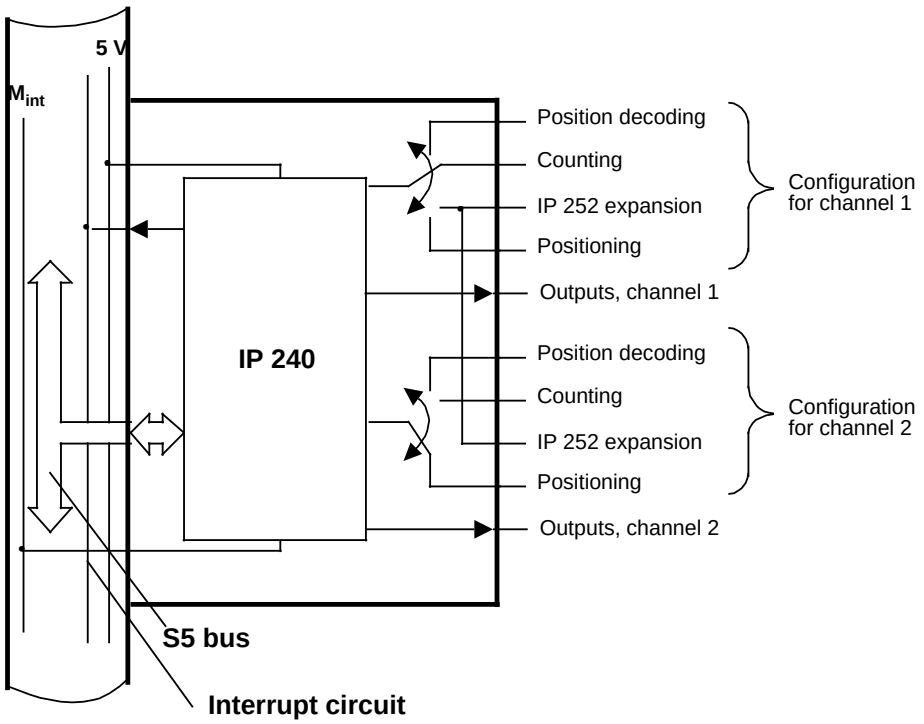
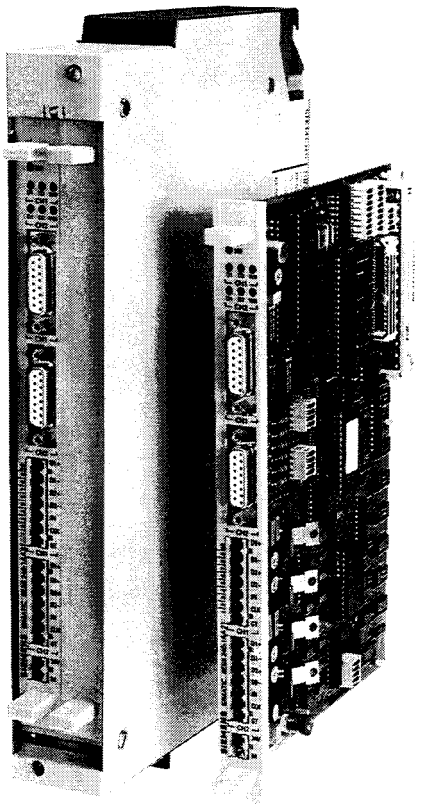


Fig. 1-1. Modes of the IP 240 Module

In the position decoding, counting and positioning modes, the IP *240* can be used as a standalone module in the U-range programmable controllers S5-115U, S5-135U (CPU 922 and 928), S5-150U and S5-155U. Operation as an expansion to the IP 252 closed-loop control module with direct data exchange between the I/O modules is only possible in the S5-115U programmable controller.

The IP 240 can be operated in the central controllers of the S5-115U, S5-135U and S5-155U and in expansion units with a central controller bus. In the S5-115U programmable controller, the compact module can be plugged in by means of an adapter casing.

Standard function blocks are available as user support for the exchange of data between the IP 240 and the S5 central processor.



g. 1-2. IP 240 with and without Adapter Casing

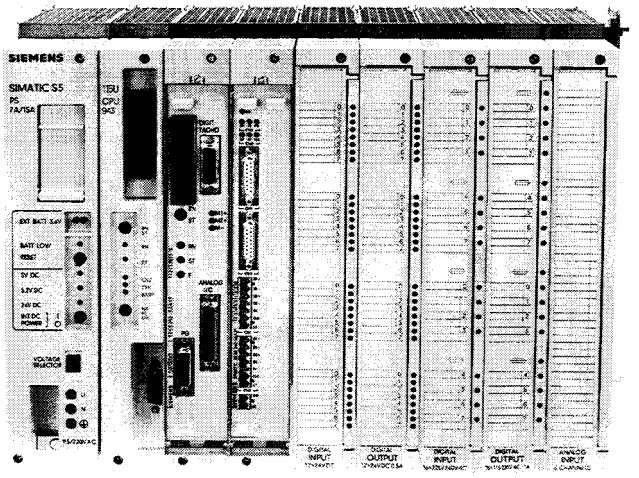


Fig. 1-3. S5-115U with the IP 240 Module

Figures

2 Module Description and Accessories

2.1 General Technical Specifications

Climatic Environmental Conditions	
Temperature	
Operation	0 to +55 °C (Intake air temperature, measured at the bottom of the module)
Storage/shipping	- 25 to + 70 °C
Temperature change	
- Operation	10 °C/h max.
- Storage/shipping	20 °C/h max.
Relative humidity	to DIN 40040 15 to 95% (indoors) noncondensing
Atmospheric pressure	
- Operation	860 to 1060 hPa
- Storage/shipping	660 to 1060 hPa

Electromagnetic Compatibility (EMC) Noise Immunity	
Damped oscillatory wave test (1 MHz)	to IEC 255-4
Digital-inputs and outputs	1 kV
Static electricity	to IEC 801-2 (discharge on all parts accessible to the user during normal operation)
Test voltage	3 kV
Radiated electro-magnetic field test	to IEC 801-3 Test field strength 3 V/m
Fast-transient burst test	to IEC 801-4
Digital-inputs and outputs	1 kV

Mechanical Environmental Conditions	
Vibration	to IEC 68-2-6
- Tested with	10 to 57 Hz, (constant amplitude 0.15 mm)
	57 to 150 Hz, (constant acceleration 2 g)
Shock	IEC 68-2-27
-Tested with	12 shocks (semisinusiodal 15 g/11 ms)
Free Fall	IEC 68-2-32
- Tested with	Height of fall 1 m

Specifications on IEC/VDE safety	
Degree of protection	to IEC 529
- Implementation	IP 20
- Class	I to IEC 536
Insulation rating for the digital outputs	to VDE 0160
- Nominal insulation voltage between electrically independent circuits **and** circuits connected to central ground	30 V DC
Test voltage at a rate voltage U_e of the AC or DC circuit of U_e=0 to 50 V	sinusoidal, 50 Hz 500 V

2.2 Technical Specifications

The IP 240 has two independent channels.

In the **IP 252 expansion** mode, the encoder signals are acquired as in the position decoding and positioning modes. The data relating to pulse inputs for position decoding therefore also apply to the **IP 252 expansion**.

Current consumption, internal	Max.	0.5 A at 5 V without encoder supply
Weight	Approx.	450 g
Width of the module		1 SPS=20 mm

2.2.1 Position Decoding and Positioning

Pulse inputs	
Encoders	Incremental encoders with the following characteristics:
- Encoder signals	Two pulse trains displaced by 90 ° (Channels A and B), one reference signal (Channel Z) The Z signal is evaluated in zero mark monitoring and reference point approach during signal state A="1" and B="1". For the duration of signal Z, states A="1" and B="1" may only occur once (Section 13.1.1).
- Encoder output circuits	with **symmetrical pulse train** to RS 422 A or similar, rated encoder voltage 5 V, connection to inputs: A and $\overline{A}$, B and $\overline{B}$, Z and $\overline{Z}$
	with **asymmetrical pulse train**, e.g. push-pull, open collector (external pull-up resistors required), rated encoder voltage 5 V or 24 V, connection to inputs: A*, B*, Z*
Binary input	
Encoders	e.g. BERO proximity switches
- Encoder output circuit	Switching to P potential Operating voltage 5 V or 24 V, connection to input: IN (preliminary contact)

Input frequencies

Pulse inputs:

- Symmetrical signals	max. 500 kHz	in position decoding and positioning mode
	max. 200 kHz	in IP 252 expansion mode
- Asymmetrical signals		
5 V [1]	max. 50 kHz	
24 V [2]	max. 25 kHz	for 100 m cable
	max. 50 kHz	for 25 m cable
Binary input:	max. 100 Hz	

2.2.2 Counting

Pulse input

Encoders	e.g. incremental encoders
- Encoder output circuit	Switching to P potential, encoder voltage rating 5 V or 24 V, connection to input: CLK (clock)

Binary input

Encoders	e.g. BERO proximity switches
- Encoder output circuit	Switching to P potential, operating voltage 5 V or 24 V, connection to input: GT (gate)

Input frequencies

Pulse input:	5 V [1]	max. 70 kHz
	24 V [2]	max. 25 kHz for 100 m cable
		max. 70 kHz for 25 m cable
Binary input:	max. 100 Hz	

---

[1] max. encoder output resistance 330
max. capacitance per unit length of cable 100 pF/m

[2] max. encoder output resistance 1 k
max. capacitance per unit length of cable 100 pF/m

Encoder output circuit series-mode

2.2.3 Inputs/Outputs

The IP 240 provides two options for connecting sensors to the pulse inputs:
- All sensor signals can be routed to the 15-pin subminiature D socket connectors X2/X4 (Section 4.2.2)
- Clock signals up to 10 kHz can also be routed over the 7-pin plug connectors X3/X5 (Section 4.2.2).

The sensor power supply is only available at the 15-pin subminiature D socket connectors.

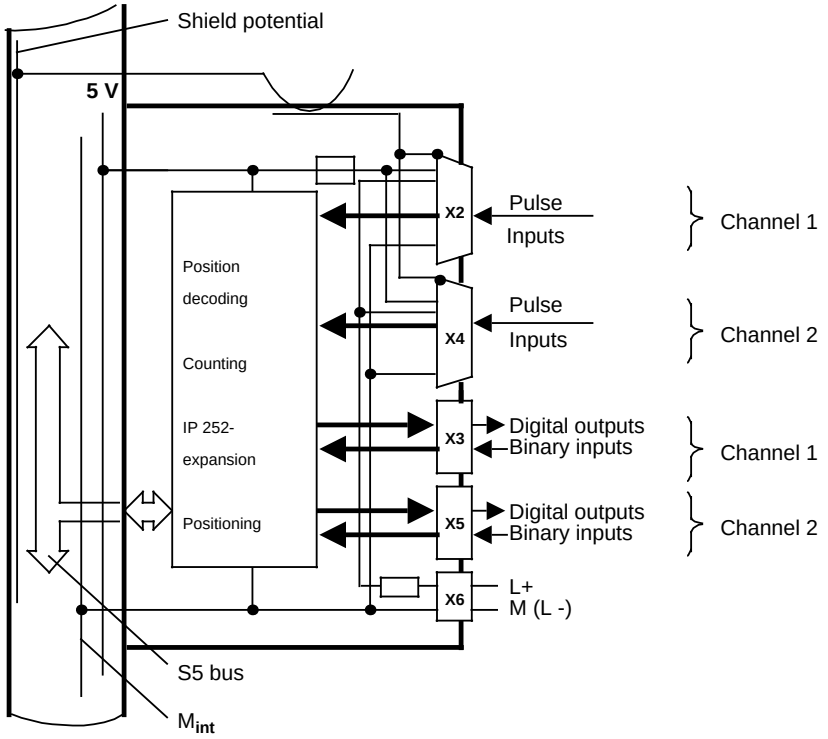


Fig. 2-1. Front Connectors

Warning

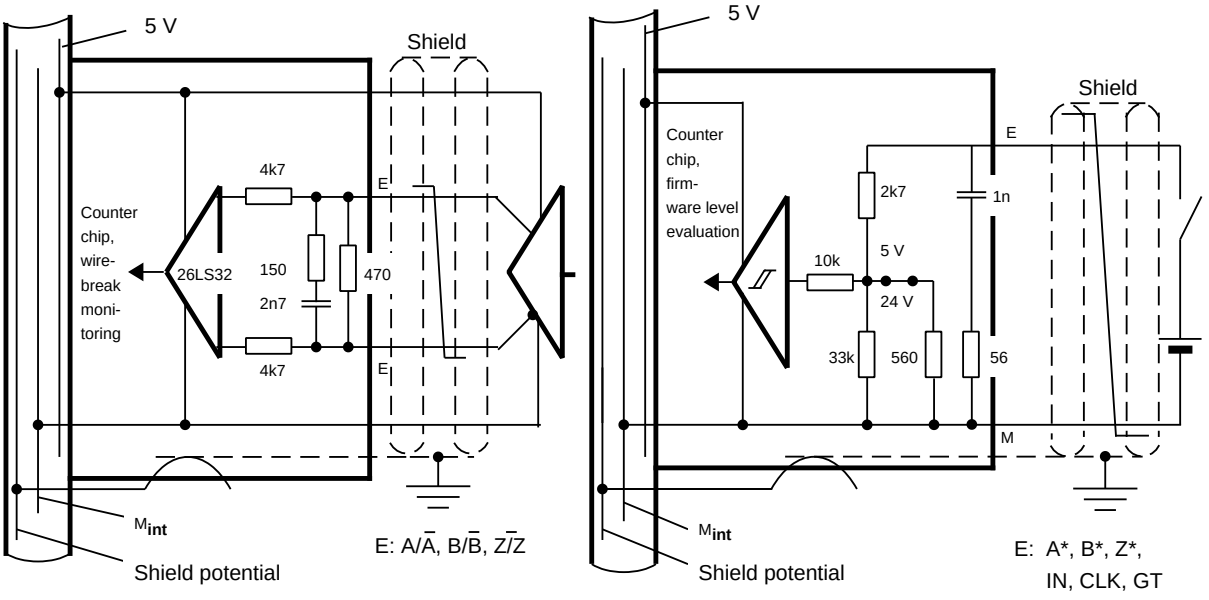
To ensure noise immunity, all inputs, outputs and the 24 V supply on the IP 240 must be connected using shielded, twisted-pair cables.

Terminal M (L-) is connected on the IP 240 to the module ground (M_{int}).

Inputs

Terminals	A and $\overline{A}$ B and $\overline{B}$ Z and $\overline{Z}$	A* B* Z*	IN (prelim. contact) CLK (CLOCK) GT (GATE)
Encoder signals	Symmetrical (RS 422 A)	Asymmetrical	
Rated voltage	5 V	5 V or 24 V	5 V or 24 V
Galvanic isolation	no	no	no

Data for rated voltage	5 V sym pulse train A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$	5 V A*, B*, Z* IN, CLK, GT	24 V A*, B*, Z* IN, CLK, GT
Input voltage ranges ”0”-Signal ”1”-Signal	to RS 422 A	 0 ...+0.8 V +2.4 V ...+5 V	 - 30 ...+ 5 V +13 ...+ 30 V
Input currents for ”0”signal for ”1”signal for ”1”signal typ.	to RS 422 A	 - 65 ...+10 µA +90 ... +360 µA	 - 10 ...+1.6 mA +3.6 ...+ 10 mA 7.5 mA
Edge steepness of the input signals	min. 5 V/µs		
Perm. quiescent current for ”0” signal			1.5 mA
Delay time of the input circuit		4.2 µs	4.4 µs
Input resistance		36 K	3.3 k
Length of shielded and twisted-pair cable	max. 30 m (100 ft)		max. 100 m (325 ft)
Input circuit	Fig. 2.2a	Fig. 2.2b	



a) Encoders to RS 422 A (symmetrical pulse train) *b) 5 V and 24 V encoder*

Fig. 2-2. Block Diagram of the Input Circuit

Digital outputs

Number of outputs	4 (2 per channel)
Galvanic isolation	yes
in groups of	1
Supply voltage Vp	
Rating	24 V DC
Ripple	3.6 V max.
Permissible range (including ripple)	20 to 30 V
Output current for ”1” signal	0.5 A max.
Short-circuit protection	Fuse, 0.8 A fast
Voltage induced on circuit interruption limited to	- 23 V
Switching frequency	
resistive load (24 V/50 mA)	200 Hz max.
(max. 8.5 W)	2 Hz max.
inductive load (time constant max. 50 ms)	
lamp load (max. 5 W)	8 Hz max.
Simultaneity factor at 55 °C (Number of outputs simultaneously energized)	100 %
Residual current at ”0” signal	1 mA max.
Output voltage at ”1” signal	Vp - 3 V min.
Max. length of shielded twisted-pair cable	1000 m (3300 ft)
Rated insulation voltage to VDE 0160	30 V DC
Insulation group	C
tested at	500 V AC

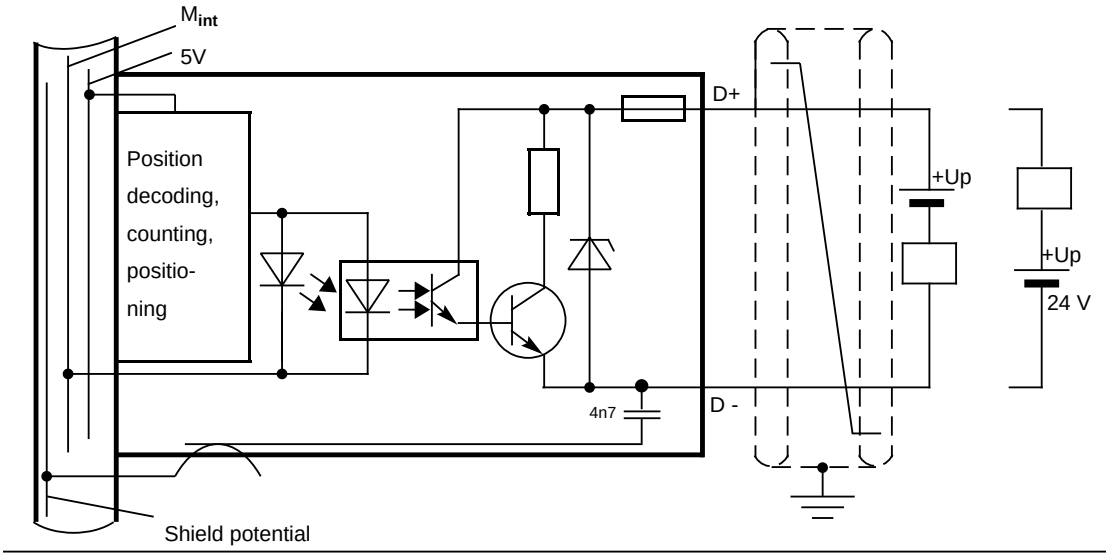


Fig. 2-3. Block Diagram of the Output Circuit

Encoder supply
The power supply for 5 V encoders is taken from the programmable controller's power supply and made available over subminiature D socket connectors X2 and X4 (pins 4 and 10) (Section 4.2.2).
If 24 V is needed, the IP 240 must be powered via the external connection on connector X6 provided for this purpose (24 V, 0 V). The 24 V input is connected internally with encoder supply outputs on subminiature D socket connectors X2 and X4 (pin 2) (Section 4.2.2). The external supply voltage is not filtered on the module.

Encoder supply

• 5 V DC	4.75 V to 5.25 V max. 0.8 A total
Short-circuit protection	Fuse 1.6 A T
• 24 V DC	20 V to 30 V max. 0.6 A total
Short-circuit protection	Fuse 1.0 A T

Influence of cable length on the encoder supply voltage
If the encoder voltage is provided by the IP 240, the voltage level and the total voltage line cross-section must be such that the voltage on the encoder lies within the stipulated tolerance.
If the supply voltage is not sufficient to supply 5 V DC for the encoder, the encoder must be provided with power from another source. The required voltage can, for instance, be fed in over the 24 V (L+)/M terminal on connector X6. Note that, when supplying incremental encoders with symmetrical outputs (to RS 422A) from another source, the difference in the earth potential between the encoder and the module electronics may be no more than ±5 V.

2.3 LEDs

LEDs display the following information:
- Hardware faults on the module (**M**odule **F**ault=**MF**),
- The states of the digital outputs (**D1** and **D2**),
- Wirebreaks and short-circuits in the encoders with symmetrical pulse trains (**W**ire-**B**reak=**WB**).

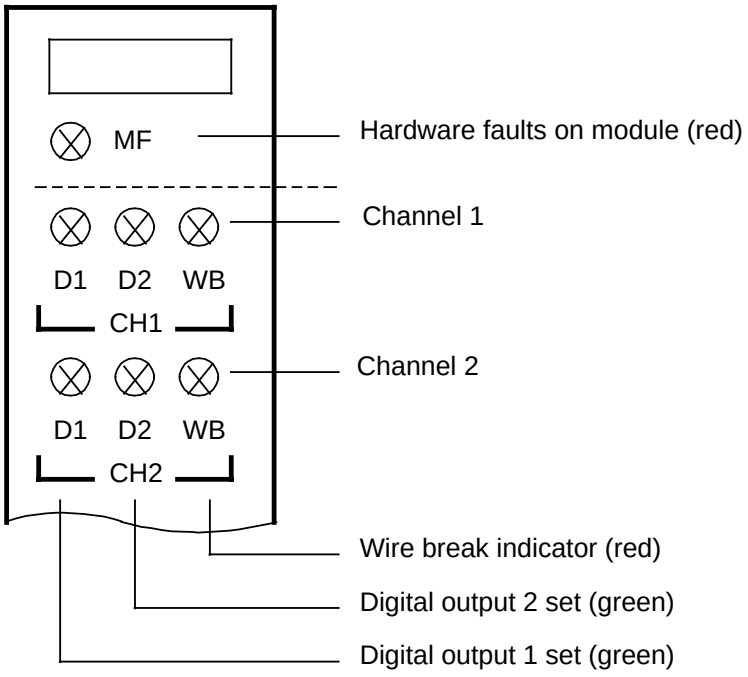


Fig. 2-4. LEDs

2.4 Order Numbers

		Order No.
Module without instruction manual		**6ES5 240-1AA21**
Adapter casing for 2 modules in S5-115U		**6ES5 491-0LB12**
Manual	English	**6ES5 998-0TB12**
”	German	**6ES5 998-0TB22**
”	French	**6ES5 998-0TB32**
”	Italian	**6ES5 998-0TB52**

Function blocks

Position decoding, counting and IP 252 expansion mode

For the S5-DOS operating system	**6ES5 848-8JB02**
For the MS-DOS/S5-DOS/MT operating system	**6ES5 848-7JB02**

Positioning mode

For the S5-DOS operating system	**6ES5 848-8JC02**
For the MS-DOS/S5-DOS/MT operating systems	**6ES5 848-7JC02**

Fuse	0.8 A F	e.g.	Wickmann No.TR5F 19370K
	1.6 A T		Wickmann No.TR5T 19372K
	1.0 A T		Wickmann No.TR5T 19374K

Position encoders with symmetrical signals
e.g. Siemens, No. 6FC9320-...

Connecting cables for 6FC9320-3..00 position decoders

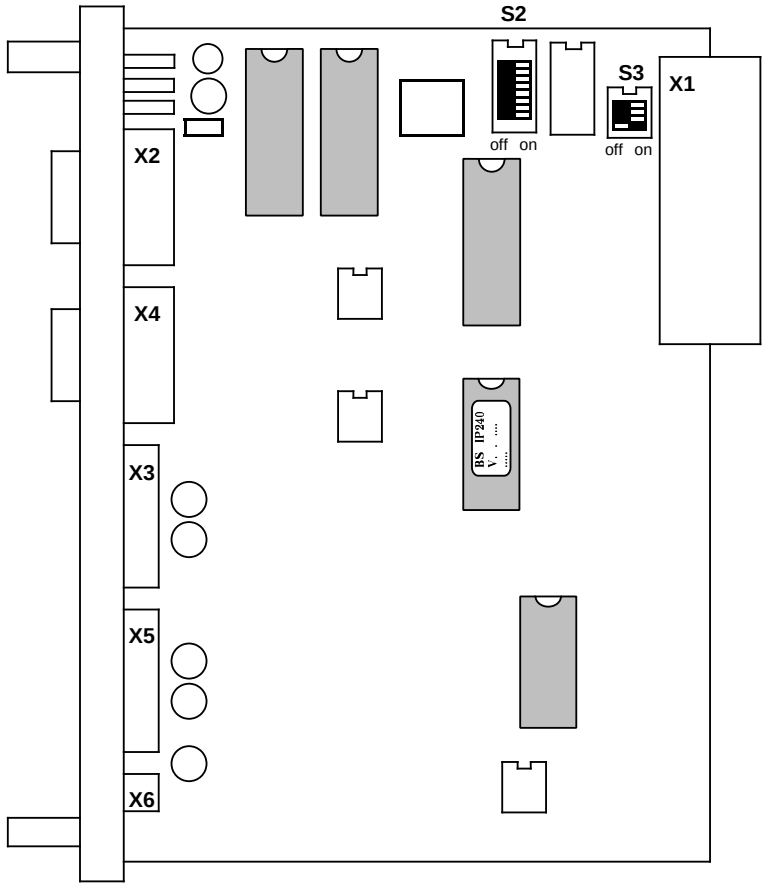
5 m	**6ES5 705-3BF01**
10 m	**6ES5 705-3CB01**
20 m	**6ES5 705-3CC01**
32 m	**6ES5 705-3CD21**

Connectors Socket connector, 2-pin (Weidmüller, BLA 12817.0)
Socket connector, 7-pin (Weidmüller, BLA 12822.0)

Figures

3 Addressing

The IP 240 module reserves an address space of 16 bytes in the I/O areas. All data are exchanged via these areas, which can be read out and written to by the S5 CPU. The data transfer is handled by a standard function block. It is merely necessary to set the desired starting address and the I/O area (P or Q area) via coding switches on switchbanks S2 and S3 on the module.
For address decoding, the IP 240 needs the memory-I/O select signal PESP in addition to the S5 bus addresses A 0 to A 11.



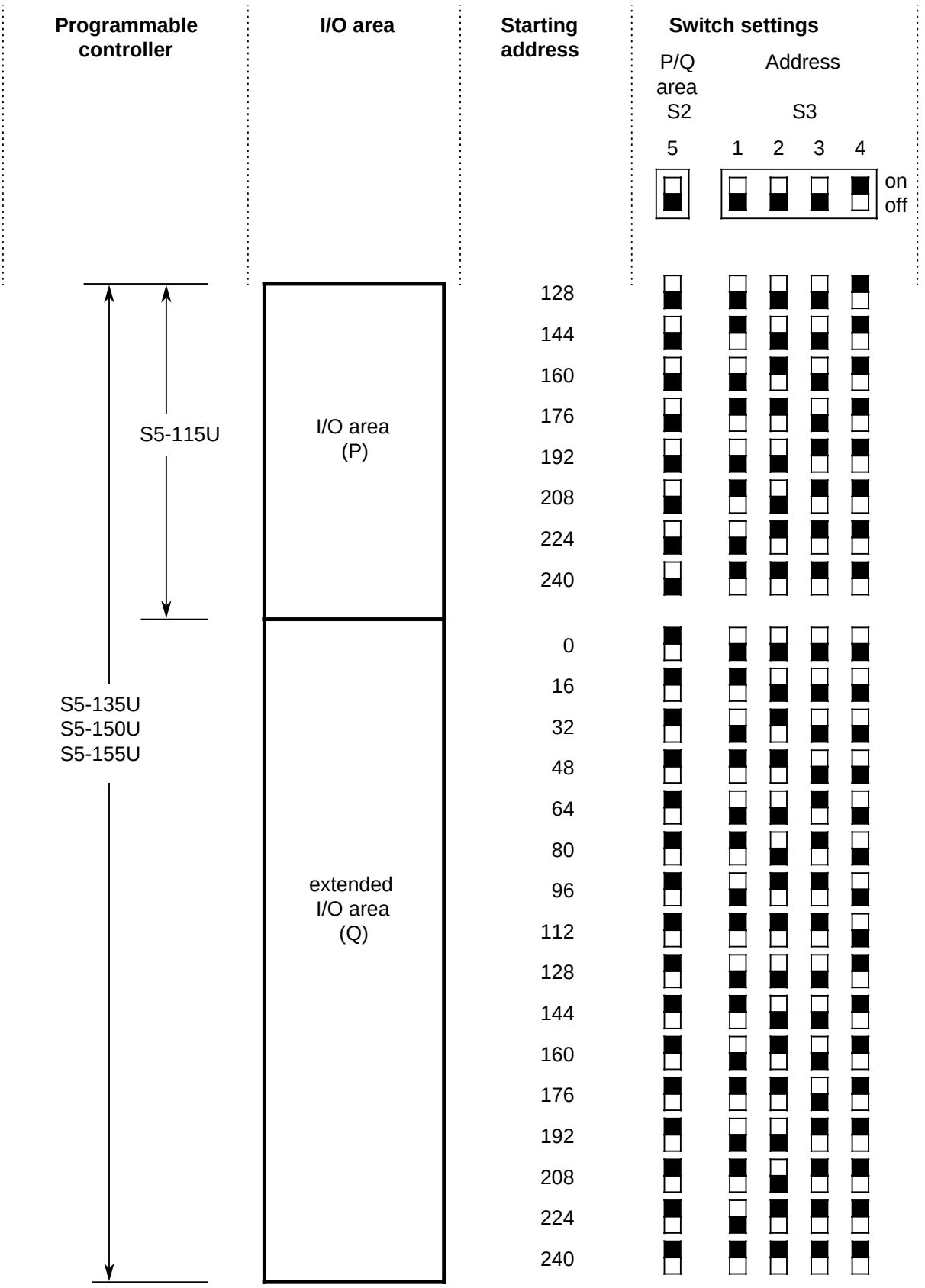
S2: Setting the address space

S3: Setting the starting address

Fig. 3-1. Locations of the Address Switches

Note

The modules are delivered with a set starting address of 128 in the normal (P) I/O area. Before start-up, make sure that no two modules reserve the same


Programmable controller
I/O area
Starting address
Switch settings
P/Q area S2
Address S3
5
1 2 3 4
on
off
S5-115U
S5-135U
S5-150U
S5-155U
I/O area (P)
extended I/O area (Q)
128
144
160
176
192
208
224
240
0
16
32
48
64
80
96
112
128
144
160
176
192
208
224
240

Use of the IP 240 in the S5-183U, S5-184U, S5-185U and S5-186U expansion units
If you use the IP 240 in one of these EUs, set the start address on switchbank S3 as explained above.

Setting the I/O area or the extended I/O area:

- S5-183U and S5-184U expansion units
  - Set the I/O area or the extended I/O area on the interface module.
  - Always put switch 2.5 on the IP in the ”off” position.

- S5-185U and S5-186U expansion units
  - Set I/O area or extended I/O area on the interface module.
  - Set I/O area or extended I/O area on the IP.

Note

The module address must lie in the P area if the IP 240 is to generate process interrupts over I/O byte PYO.

The switch 2.6 is always to be set to ”off”.

Figures

4 Hardware Installation

4.1 Installation

4.1.1 Suitable Programmable Controllers and Expansion Units

The IP 240 can be used as a compact module without fan subassembly in the following PLC central controllers:

- S5-115U with adapter casing
- S5-135U with CPU 922 (from Version 9 onwards) and CPU 928 (from 6ES 928-3UA12 onwards)
- S5-155U

The IP can also be operated in expansion units with central controller bus.

> **Note**
>
> In the S5-150U, the IP 240 can be used only in the expansion units.

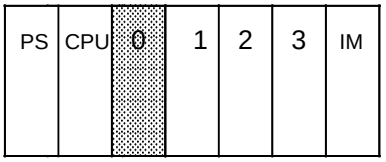
The IP is addressed over the I/O area. In the S5-115U, it can be addressed over the P area, in the other PLCs over either the P or Q area.

In the relevant central controllers and, in the case of the 115U and 155U, in expansion units 6ES5 701-3LA13 and 6ES5 186-5UA11, interrupts can be generated over interrupt circuits IRx. In this case, the 307 and 317 interface modules must be used to interconnect the expansion units.
Interrupts can be generated over I/O byte 0 in the P area only.

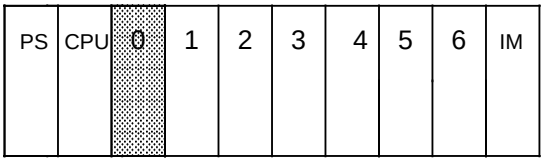
4.1.2 Permissible Module Slots

S5-115U central controller

CR 700-0 subrack

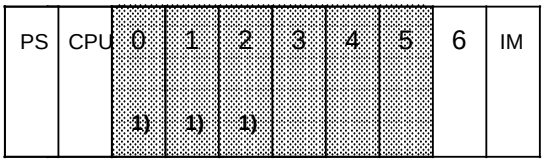


CR 700-1 subrack

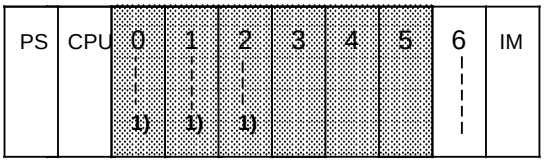


Interrupt signals $\overline{IRA}$ and $\overline{IRB}$ possible

CR 700-2 subrack



CR 700-3 subrack



The following interrupt signals can be processed:

CPU 941	$\overline{IRA}$ and $\overline{IRB}$
CPU 942, 943, 944	$\overline{IRA}$, $\overline{IRB}$, $\overline{IRC}$ and $\overline{IRD}$

1) If the IP 240 is used as IP 252 expansion, one of the following slots must be used for the associated IP 252 closed-loop control module:

CPU 941, 942, 943	Slot 0
CPU 944	Slot 0, 1, 2

S5-115U expansion unit, ER 701-3 subrack

PS	0	1	2	3	4	5	6	7	IM

Note

If the IP 240 is operated in an ER 701-3 expansion unit, interface modules 304 and 314 or 307 and 317 are required.

S5-135U central controller, MLFB 6ES5 135-3KA..

3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	155
		1)	1)	1)													1)	1)	1)	

S5-135U central controller, MLFB 6ES5 135-3UA..

3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
			1)		1)		1)										1)	1)	1)	

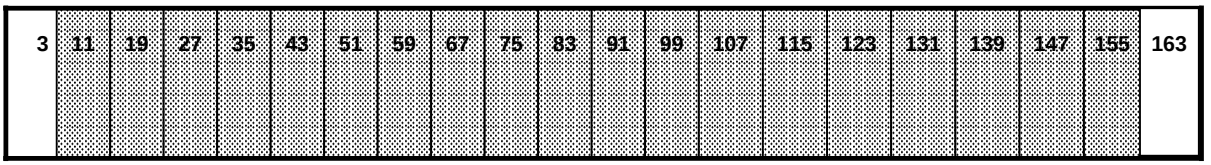
S5-155U central controller

3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123	131	139	147	155	163
		3)	3)			1)	1)	1)			1)	1)					2)	2)		

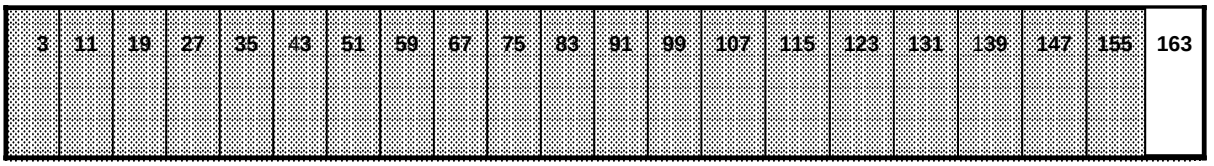
Possible slots

1) IRx interrupt signals cannot be generated in these slots.
2) Generation of IRx interrupt signals requires reconfiguring of the jumpers on the wiring backplane (S5-155U manual).
3) Only the IRA interrupt signal can be generated in these slots.

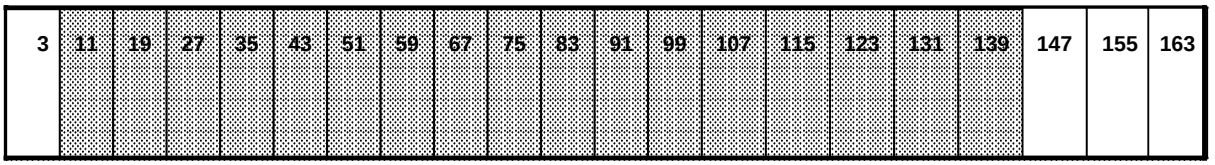
S5-183U expansion unit [1)]



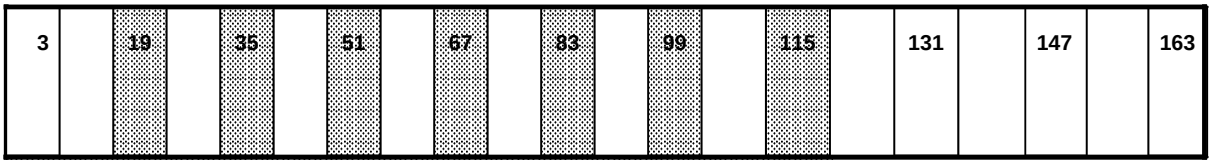
S5-184U expansion unit [1)]



S5-185U expansion unit [1)]



S5-186U expansion unit



Possible slots

1) IRx interrupt signals cannot be generated in these expansion units.

Note

When interrupts are generated over I/O byte 0, all interrupt-generating modules must be operated in either the central controller or in an expansion unit.

4.2 Wiring

4.2.1 Wiring Method

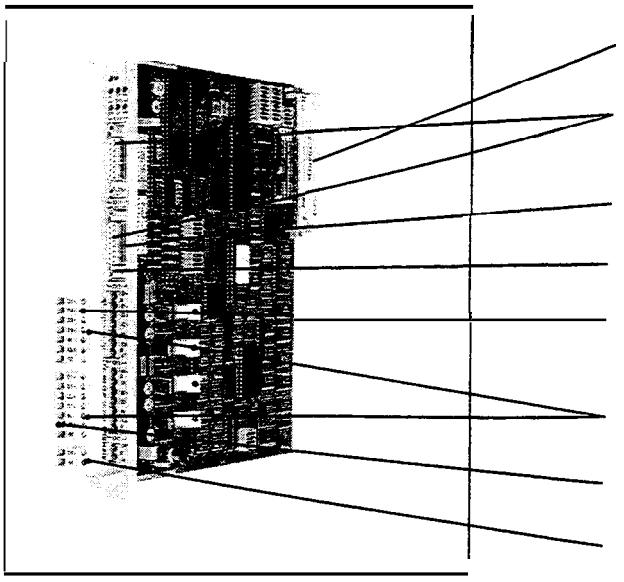


Fig. 4-1. Connectors

Permissible cross-sections of conductors

- **2 and 7-pin plug-in connector**
  - **Stranded conductor H07V-K with sleeve** — **0.5 to 1.5 mm² (20 to 15 AWG)**
  - **Solid conductor H07V-U** — **0.5to 2.5 mm² (20 to 13 AWG)**

- **Subminiature D-type connector**
  - **Flexible cable, 15-pin** — **up to 0.5 mm² (20 AWG)**

One two-pin and two seven-pin socket connectors are supplied.

Warning

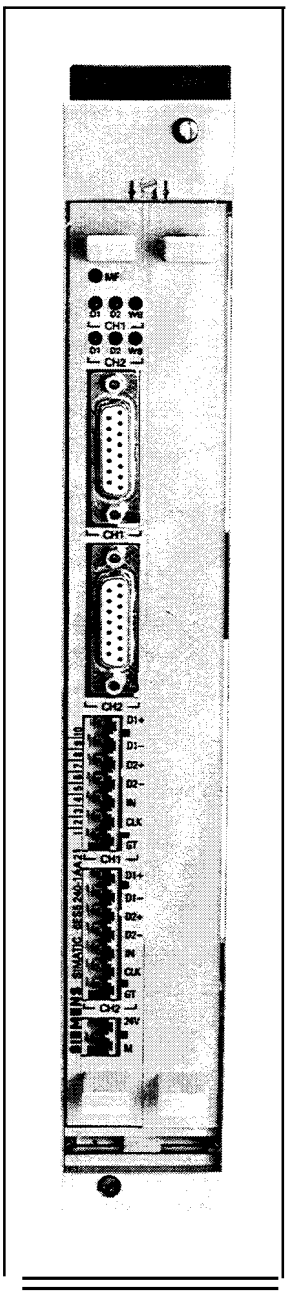
Do not plug in or unplug the module or the connector while they are under power!

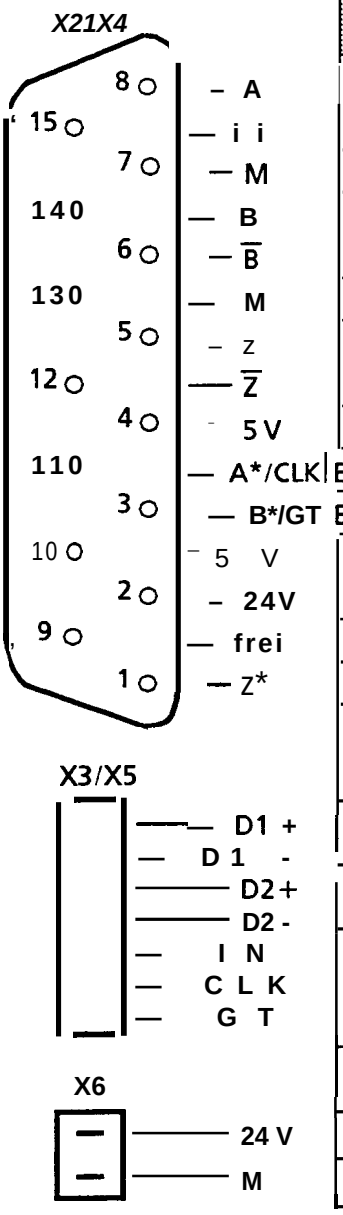
All inputs of the IP 240 are non-isolated.
Before a "1" signal can be connected to a 24 V input of the module, the chassis terminal of the IP 240 (Pin X6/M) has to be connected to the chassis terminal of the external supply.

The X6/M connection is connected to the module chassis (M_{int}) on the IP 240.

4.2.2 Connector Pin Assignments

Front Connector Pin Assignments





Position decoding IP 252 expansion Positioning	Counting
Encoder signal A, sym.	
Encoder signal $\overline{A}$, sym.	
Ground	Ground
Encoder signal B, sym.	
Encoder signal $\overline{B}$, sym.	
Ground	Ground
Encoder signal Z, sym.	
Encoder signal $\overline{Z}$, sym.	
5 V encoder voltage	
Encod. signal A*, asym.	Clock signal
Encod. signal B*, asym.	Gate signal
5 V encoder voltage	
24 V encoder voltage	24 V encod. volt.
Encod. signal Z*, asym.	
The 24 V encoder voltage is connected to the 24 V terminal on connector X6.	
Digital output 1 1)	Digital output 1
Digital output 2 1)	
Preliminary contact 1)	
	Clock signal
	Gate signal
1) Not for IP 252 expansion	
For external encoder voltage	
External signal and voltage ground	

Fig. 4-2. Connector Pin Assignments

Note

Inputs A* (X2/X4) and CLK (X3/X5) as well as B* (X2/X4) and GT (X3/X5) are connected internally.
For frequencies higher than 10 kHz, counting pulse encoders must be connected via the subminiature D socket connector.
if you use a 5 V encoder, you must apply the 5 V supply voltage to pins 4 and 10 to keep voltage drops on these supply lines to a minimum. The ground must be connected to pins 7 and 13.

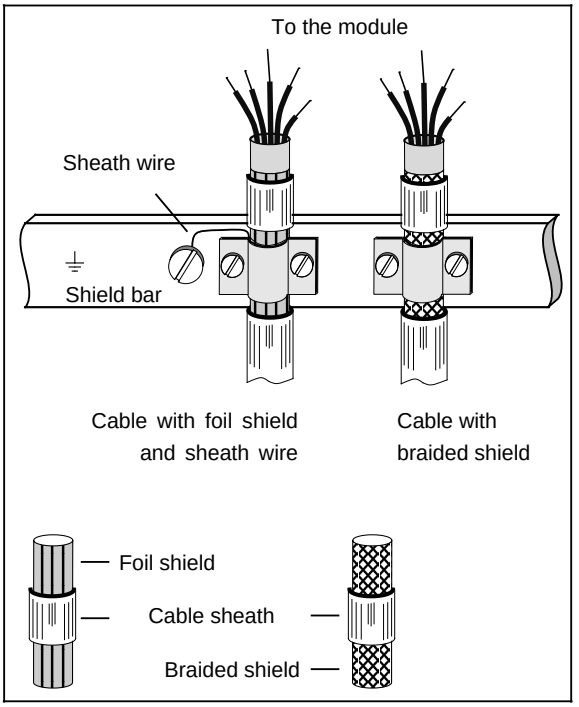
Shielding of cable connections on the IP 240

Warning

To ensure noise immunity, shielded twisted-pair cables must be used for all IP 240 connections (inputs, outputs, 24 V power supply).

The following applies to shielding of the connecting cables:

- .The cable shields must be placed on a shield bus near the cable entry in the cabinet.
- Braided shields must be secured over as large an area as possible direct to the shield bus (for instance with metal cable clamps which span the shield).
- When using cables with foil shields, the sheath wire incorporated in the shield must be connected through as short a path as possible (less than 3 cm) to the shield bus.
- The shielding must be extended from the shield bus to the module.
- The shield bus must be conductively connected to the supporting bar, the cabinet, and the central grounding point in the cabinet.
- The section entitled ”Installation Guidelines” in the S5-115U Manual, Edition 2, provides detailed information on grounding the cable shields.



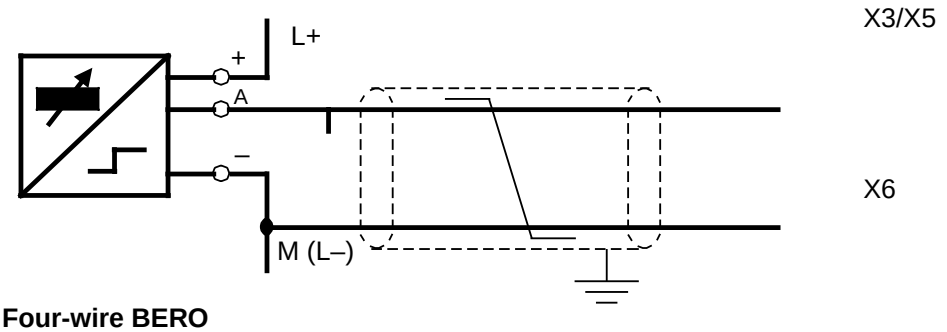
Pin assignments for base connector X 1

d	b	z	Pin-Nr.
	M	+5 V	2
	PESP		4
	ADB 0	RESET	6
	ADB 1	MEMR	8
	ADB 2	MEMW	10
	ADB 3	RDY	12
IRA	ADB 4	DB 0	14
IRB	ADB 5	DB 1	16
IRC	ADB 6	DB 2	18
IRD	ADB 7	DB 3	20
	ADB 8	DB 4	22
	ADB 9	DB 5	24
	ADB 10	DB 6	26
	ADB 11	DB 7	28
	BASP		30
	M		32

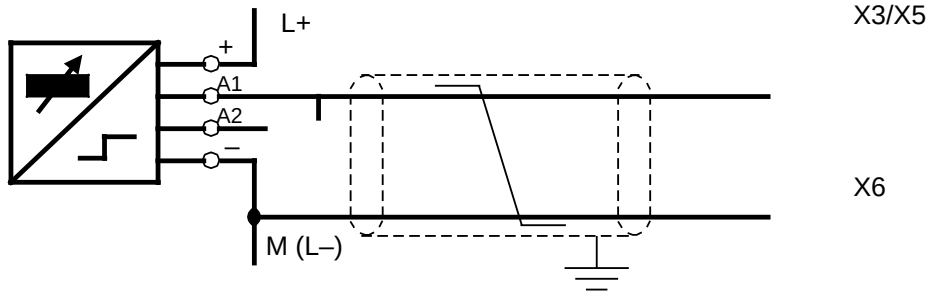
4.3 Installation Examples

4.3.1 Inputs

Three-wire BERO



Four-wire BERO



A1 has NO function ("1" signal)
A2 has NC function ("0" signal)

Fig. 4-3. Connection of BERO Proximity Switches

> **Note**
>
> Only inductive proximity switches with outputs switching to L+ potential can be connected to the 24 V inputs of the module.
> All inputs connected to BEROs must be set to 24 V (switches S5 and S6, Section 5.3.2).
> The encoder ground must be directly connected to the module ground.

Incremental Encoders
(with symmetrical outputs to RS 422 A)

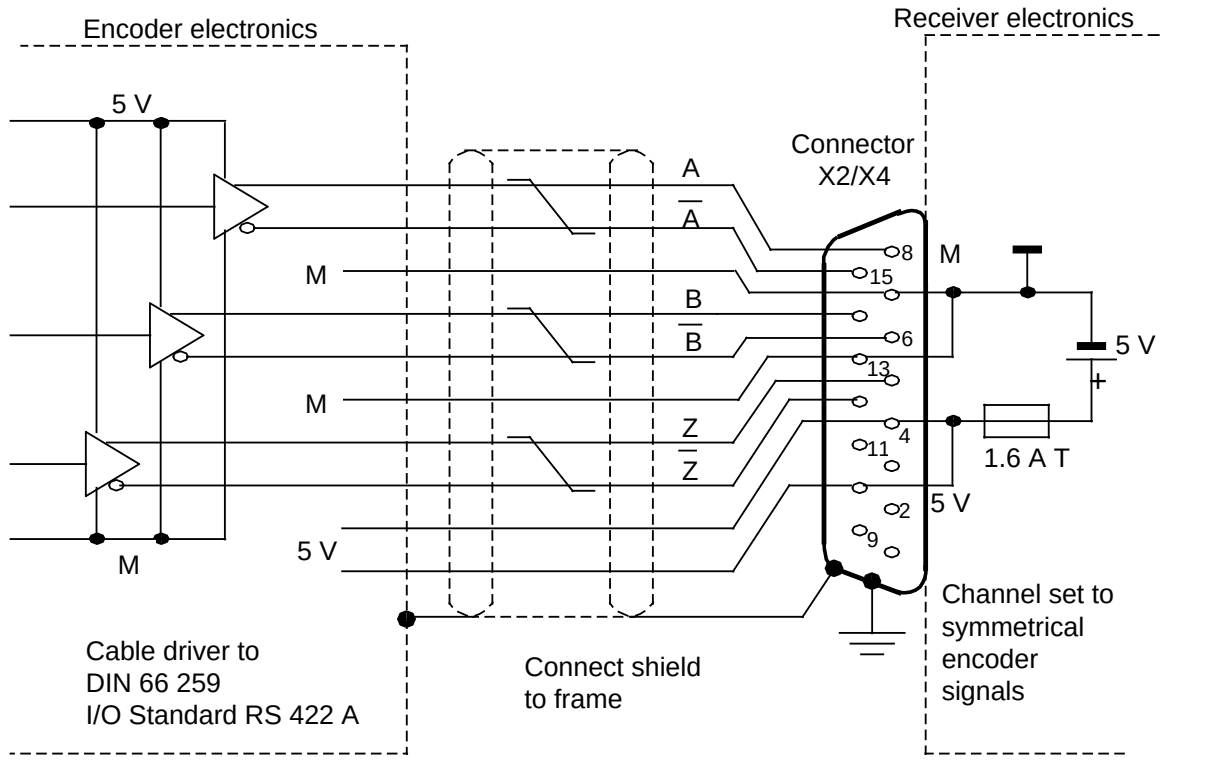


Fig. 4-4. Connection of Encoders with Symmetrical Output Signals

Note

An AM26LS32 line receiver is used in the receiver electronics. The maximum permissible cable length is 30 m (100 ft.).
If the encoder electronics are operated with an independent supply (5 V), ground potential differences of ±5 V between encoder electronics and receiver electronics are permissible.
To change the direction of counting, A/$\overline{A}$ and B/$\overline{B}$ must be interchanged.

Incremental Encoders
(with asymmetrical outputs)

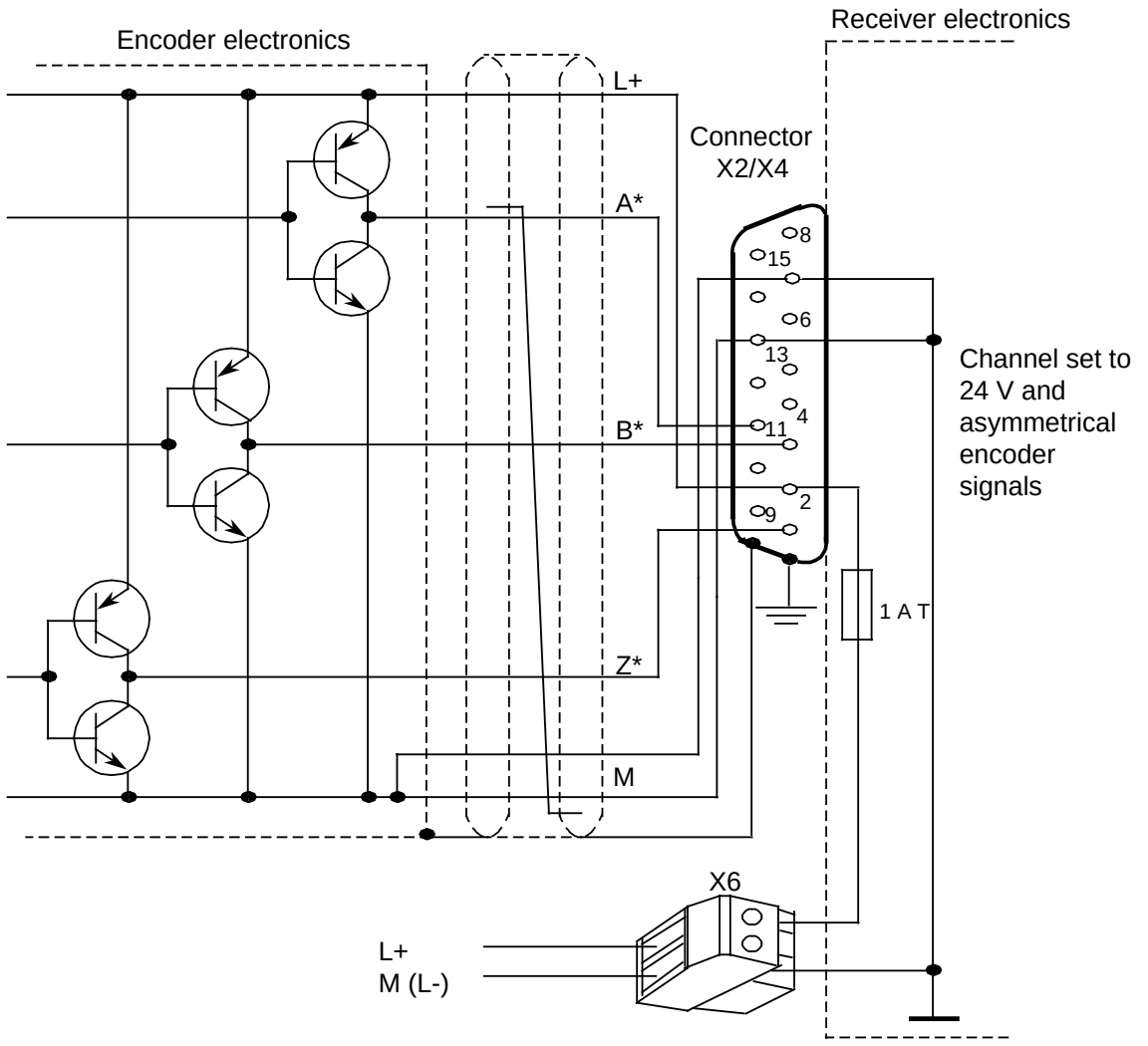


Fig. 4-5. Connection of Encoders with Asymmetrical Signals: Push-Pull Encoder Output Circuit

Note

Ground connection M(L-) must have as low a resistance as possible.

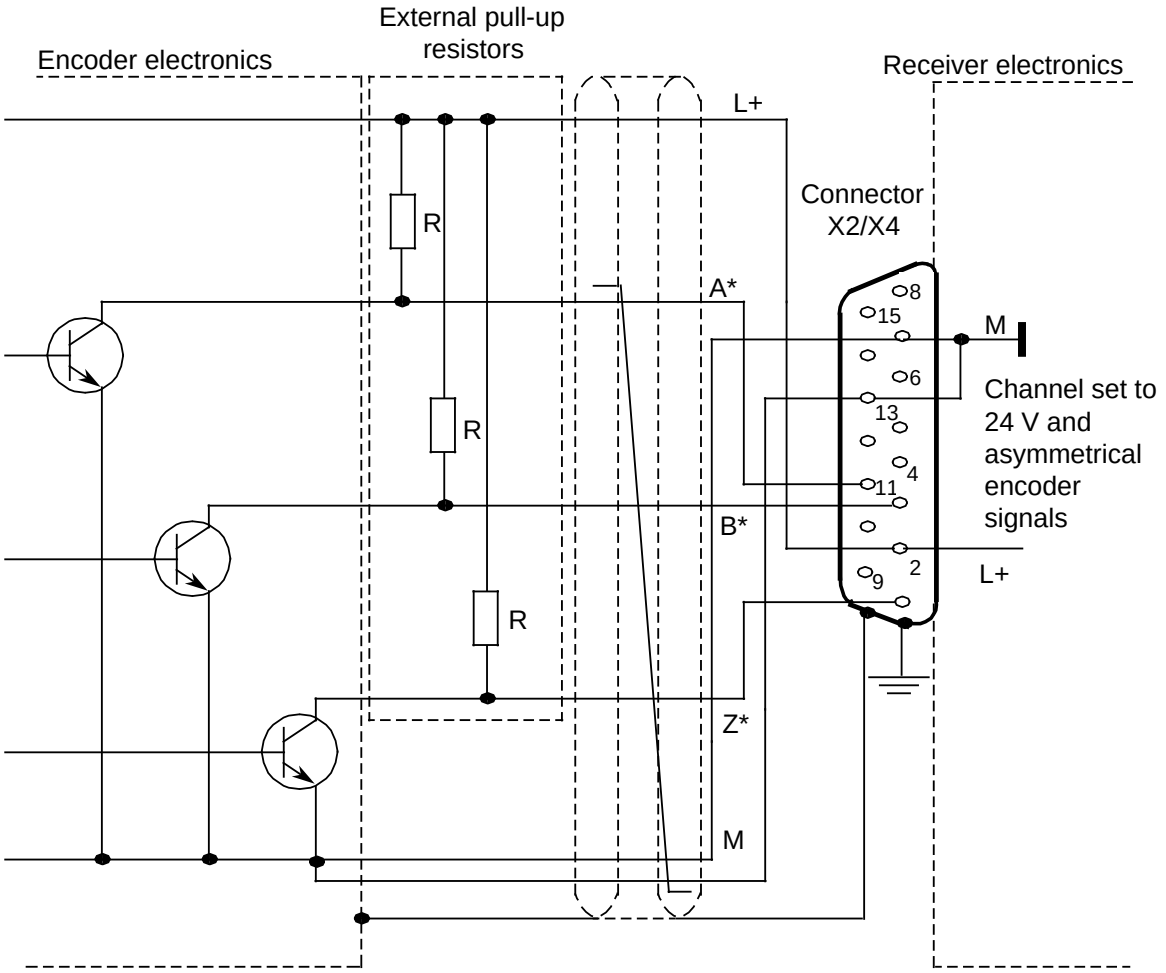


Fig. 4-6. Connection of Encoders with Asymmetrical Signals: Open-Collector Encoder Output Circuit

Note

All encoders whose output circuitry allows a load with respect to ground and meets the required input level can be connected.
Encoders with open-collector outputs can also be connected with external pull-up resistors.
To change the direction of counting, A* and B* must be interchanged.

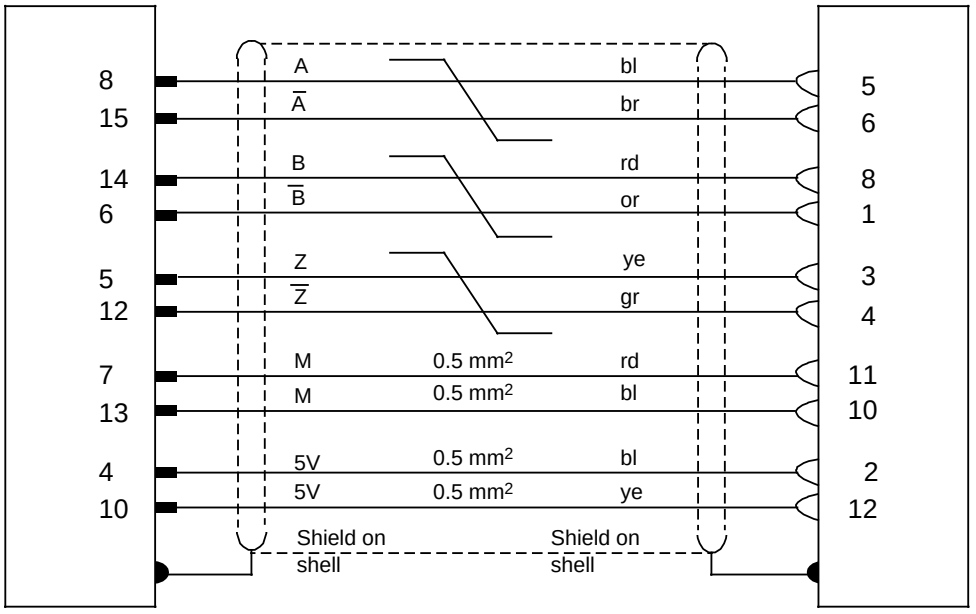
SIEMENS provides the following prefabricated cables for connecting a 6FC9320-3..00 incremental encoder to the IP 240:

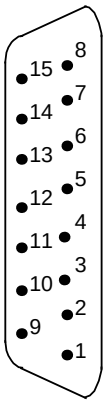
Cable designation : IP 240 pulse encoder (6FC9320-... with SIEMENS circular connector)
Order No. : 6ES5 705-3xxx1

xxx = Length code
5 m BF0
10 m CB0
20 m CC0
32 m CD2

For other lengths, see Catalog ST 52.3 or ST 54.1 .

The diagram below shows the connector pin assignments.





15-pin subminiature D
plug connector
wiring post side
metal-plated shell
with screw clamp
6FC9341- 1HC

12-pin
circular socket
wiring post
side
6FC9341-1FD

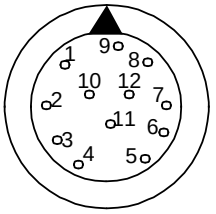
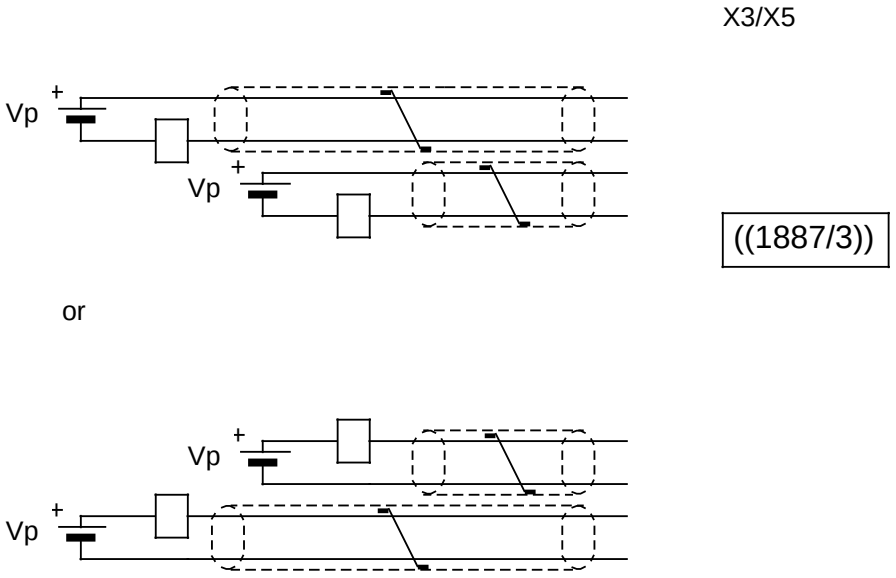


Fig. 4-7. Pin-Out Diagram for 6ES5 705-3xxx1 Connectors

4.3.2 Outputs



Vs=Supply voltage

Fig. 4-8. Connecting the Load to the Digital Outputs on the IP 240

> **Note**
>
> All digital outputs are isolated from each other and from the module ground.

> **Warning**
>
> Because of internal protective diodes, if the cables to D+ and D - are connected the wrong way round, the outputs are bypassed. Any supply voltage is then switched directly to the load.
>
> In order to avoid noise voltages, relays and contactors have to be connected with arc suppression devices.

Figures

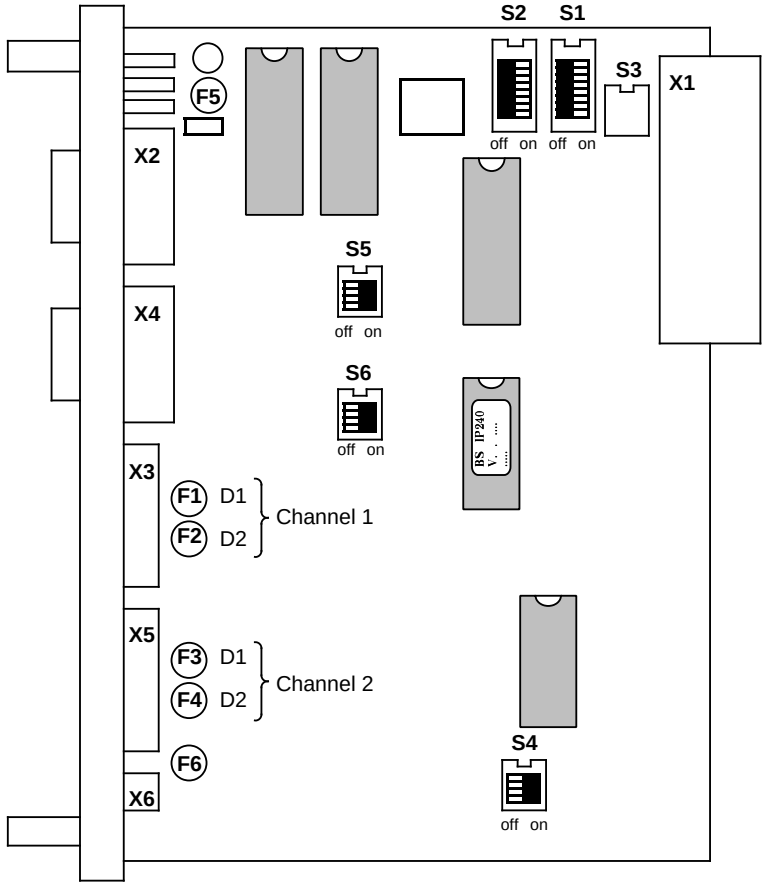
Tables

5 Operation

Before startup you must set various coding switches on the module.
You can stipulate

- interrupt generation with switchbanks S1 and S2 (Section 5.1)
- disabling of the digital outputs in the event of active BASP signal with switchbank S4 (Section 5.2)
- encoder signal matching with switchbanks S5 and S6 (Section 5.3)

The locations of the switchbanks and the fuses are shown in Fig. 5-1. The switch settings in the figure are factory setttings.



S1: Setting assignments in PB0 (Chapter 5.1.2)

S2: Setting interrupt generation (Chapter 5.1)
Setting address range (Chapter 3)

S4: Setting sensor type sym./asym. (Chapter 5.3.1)
Setting response to BASP (Chapter 5.2)

S5/S6: Setting the sensor signal level for channel 1 (S1) and channel 2 (S6) (Chapter 5.3.2)

F1 ... F4: Fuses for digital outputs

F5: Fuses of the 5 V sensor supply

F6: Fuse of the 24 V sensor supply

Fig. 5-1. Locations of Switchbanks and Fuses

5.1 Settings for Interrupt Generation

The processing of interrupt signals makes it possible to respond rapidly to status changes.
In the SIMATIC S5 programmable controllers, a distinction is made between two types of interrupts:

- "Servicing IRx interrupt circuits" (S5-115U, S5-135U and S5-155U in the 155U mode)
- "Reading I/O byte 0" (S5-150U and S5-155U in the 150U mode).

5.1.1 IRx Interrupt Circuits

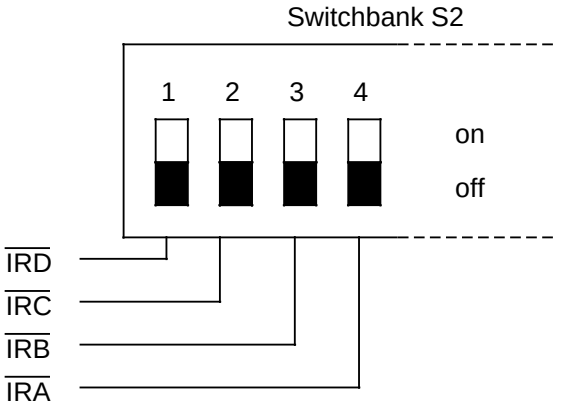
The interrupt signal generated on the IP 240 can be routed to the S5-CPU via one of four interrupt circuits $\overline{IRA}$ to $\overline{IRD}$ for interrupt processing. The following must be taken into account:

- the possible slots on the IP 240 (Section 4.1.2)
- the capabilities of the programmable controllers and individual CPUs (Table 5-1)
- the required switch settings on the IP 240

Table 5-1. Allocation of Serviceable Interrupt Circuits

PLC	CPU	CPU slot	Serviceable interrupt circuit
S5-115U	941		$\overline{IRA}$, $\overline{IRB}$
	942, 943, 944		IRA, IRB, IRC, IRD
S5-135U	922 or 928	11	$\overline{IRA}$
	922 or 928	19	$\overline{IRB}$
	922 or 928	27	$\overline{IRC}$
	922 or 928	35	IRD
S5-155U (155U mode)	946/947, 922 or 928	11	$\overline{IRA}$
	946/947, 922 or 928	51	$\overline{IRB}$
	922 or 928	91	$\overline{IRC}$
	922 or 928	99	IRD

Allocation of coding switches on switchbank S2 to the IRx interrupt circuits
Use coding switches S2.1 to S2.4 to set the IRx interrupt circuit to be used.



Coding switches S2.1 to S2.4
on : the corresponding interrupt circuit is used
off: the corresponding interrupt circuit is not used

Fig. 5-2. Allocation of Coding Switches on Switchbank S2 to the IRx Interrupt Circuits

If several IP 240 modules use one interrupt circuit, the current interrupt source must be determined by reading the interrupt request bytes of all modules or by additionally evaluating I/O byte 0. This must be taken into account in the STEP 5 program due to the system characteristics of the S5-115U CPUs (Section 5.1.2).

Note

- In the S5-115U, S5-135U and S5-155U, only one of the coding switches S2.1 to S2.4 may be closed at any given time. In the S5-150U, these switches must always be set to ”off”.
- If the 6ES5 434-7LA11 digital input module is used in the S5-115U, interrupt circuit IRA is already reserved and is no longer available for IP 240 modules.
- In the S5-135U, interrupt-driven program processing must be level-triggered (this corresponds to the basic settings in DX 0).
- In the S5-155U (155U mode), the selected interrupt circuit must be set on the CPU 946 and enabled additionally in DX 0.

5.1.2 I/O Byte 0 (PY)

In the S5-150U and S5-155U programmable controllers (in the 150 U mode), an interrupt request from up to eight modules is detected by reading I/O byte 0. Evaluation of I/O byte 0 in IP 240 modules is possible only when theses modules are addressed in the P area.

For interrupt generation over an IRx interrupt circuit, the **additional** evaluation of I/O byte 0 enables the use of one interrupt circuit for several IP 240s.

Interrupt generation with I/O byte 0
Each bit in I/O byte 0 can be reserved by **one** module with interrupt capablity. Switches **S1.1 to S1.8** on switchbank S1 are available on the IP 240 for this purpose. By defining which bit is to be set for an interrupt signal on the module, the priority can be determined with which the interrupt request is processed if two or more interrupt requests are pending simultaneously. Bit 0.0 has the highest priority and bit 0.7 the lowest.

The module with the highest priority (I/O byte 0.0) is declared to be the master module of the programmable controller. It is used to mask all unassigned bits of I/O byte 0. If an IP 240 is used as the master module, switch S1.1 must be closed (”on” position). To mask the unassigned bits in the I/O byte 0, the corresponding switches on the switchbank S1 have to be set to ”on”.

On the remaining IP 240 modules, designated as slaves, the switch for the corresponding bit in I/O byte 0 and switch **S2.7** must be closed ("on" setting). All other switches on bank S1 must be set to the ”off” position.

Switch **S2.8** must be closed on both master and slave modules to enable interrupt generation via the I/O byte 0. Only then does the IP 240 make data available when the S5 CPU reads I/O byte 0.

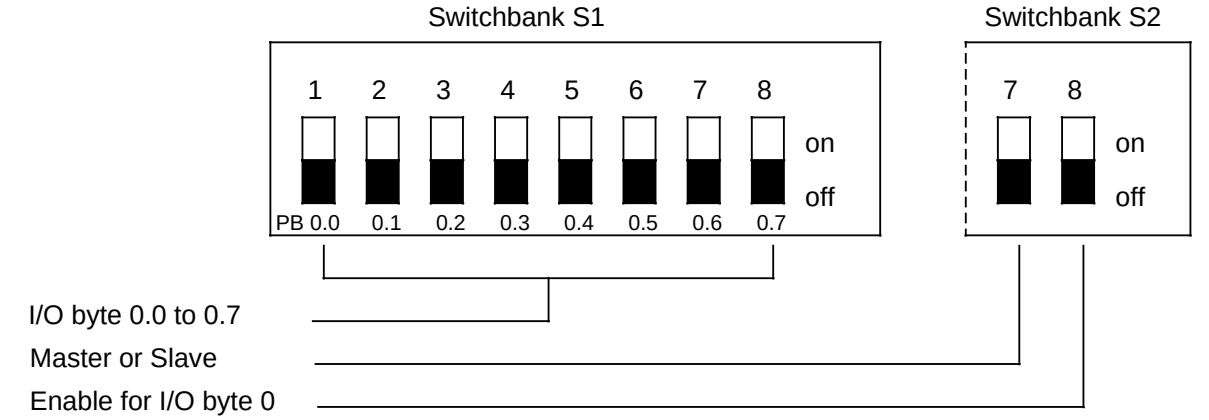


Fig. 5-3. Allocation of Coding Switches on Switchbanks S1 and S2 to Interrupt Generation with I/O Byte 0

The coding switches on banks S1 and S2 shown in Fig. 5.3 have the following meaning:

on: The corresponding bit of I/O byte 0 is set in response to an interrupt signal on the I/O module. And on a master module: the corresponding bit of I/O byte 0 is not reserved by a slave module.

on: The I/O module is operated as slave
off: The I/O module is operated as master

on: Enabling of interrupt generation over I/O byte 0

Note

No input module may be set to address IB 0 when I/O byte 0 is enabled with switch S2.8.

In the S5-155U, process interrupt generation via I/O byte 0 must also be enabled in DX 0.

Calling the interrupt OBs in the S5-150U and S5-155U (150 mode)
In the S5-150U and S5-155U (150 mode), a change in one of the bits in I/O byte 0 invokes the corresponding interrupt OB at the next block boundary. When you initialize the module with function blocks 167, 169, and 171 (Sections 10.23.2, 7.3.1 and 8.3.1), you can set the ABIT parameter to specify whether the interrupt OB is to be invoked after every signal change or only when the bit goes from 0 to1.

ABIT parameter:

ABIT : KY x,y

- x>0 : The interrupt OB is invoked on every signal change.
- x=0, y=0 to 7 : The interrupt OB is invoked only on a signal change from 0 to 1. Y is the number of the bit in I/O byte 0 which you have set on switchbank S1.

Example for setting the coding switches
Three IP 240s are to be enabled for interrupt generation. One IP 240 is to be operated as master module and the other two as slave 1 and slave 2. Slave 1 is assigned to PY 0.1 and slave 2 to PY 0.2. Bits PY 0.3 to PY 0.6 are reserved by other modules. PY 0.7 is not used and must be masked on the master module or else OB9 must not be programmed.
Fig. 5-4 shows the necessary settings of coding switches on the IP 240 modules.

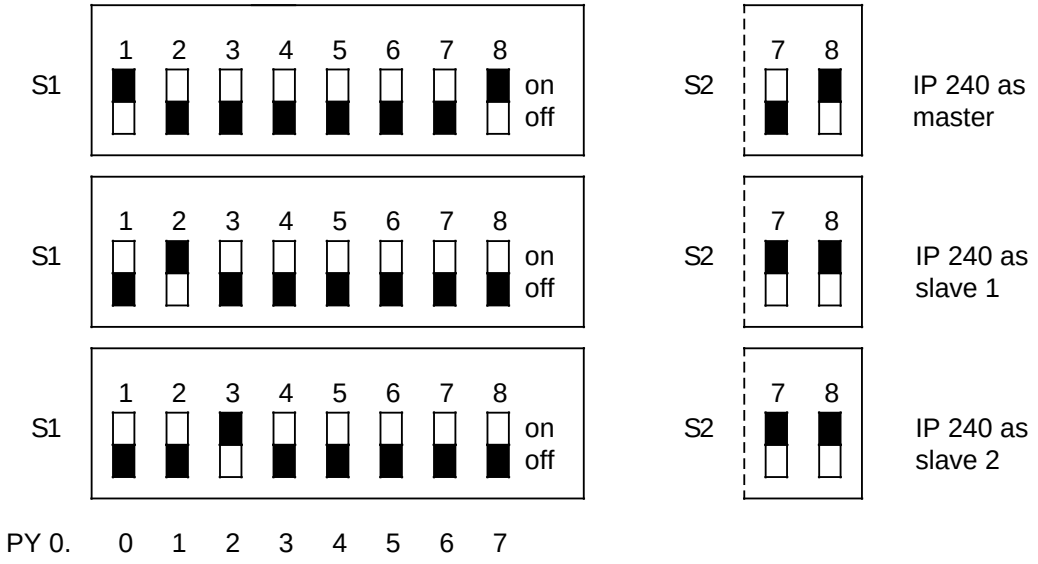


Fig. 5-4. Settings of the Coding Switches (Example)

If slave 1 and slave 2 generate a process interrupt, the value 06_H is stored in PY 0.

Additional evaluation of I/O byte 0 for interrupt generation over the IRx interrupt circuit (S5-115U, S5-135U and S5-155U (155 mode))
I/O byte 0 on the IP 240 can also be scanned when the interrupt is generated over interrupt circuit IRx. Additonal evaluation of I/O byte 0 makes it possible to operate several IP 240s on a single interrupt circuit. When this option is used, however, I/O byte 0 may not be reserved by any other module.

Required switch settings on the IP 240:
- Use the coding switches on bank S1 to determine which bit in I/O byte 0 is to be reserved. (Switch S1.1 corresponds to bit 0.0 etc.)
- Close switches S2.7 and S2.8 (”on” position)

After reading I/O byte 0, only those bits reserved by the IPs must be evaluated.

Additional programming in the organization blocks for the S5-115U:

a) The interrupt service routine must be programmed in an FB so that it may execute several times.

- I/O byte 0 must be read once at the beginning of interrupt processing to determine which IP triggered the interrupt.
- I/O byte 0 must also be read at the end of the interrupt service routine. If a new interrupt request is pending, it must be serviced without exiting the interrupt OB.

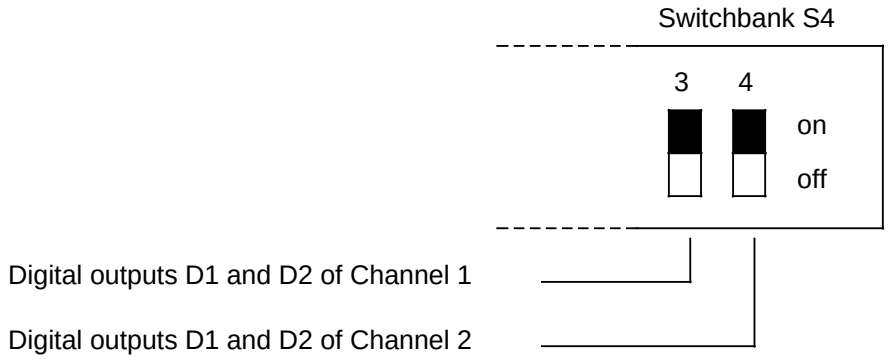
> **Warning**
>
> Failure to include these steps in the STEP 5 program will block all further interrupt generation on this circuit should a single interrupt fail to be serviced.

b) So that the CPU does not go to the stop state with a time-out, the following sequence of statements must be inserted into OB21 and OB22.

STL OB21 and O 22	STL FBn	Explanation
JU FBn NAME: XYZ ... BE	L RS 16 L KH FEFF AW T RS 16 BE	This sequence of instructions prevents updating of word 0 in the process input image.

5.2 Output Inhibit (BASP)

If the S5 CPU goes to the stop mode, this does not affect the IP 240 firmware; the module continues to run in the specified mode and can also activate the digital outputs when the programmable controller is at stop. However, all digital outputs on the IP 240 can be deenergized with an output inhibit (BASP) signal generated by the S5 CPU in the STARTUP and STOP states.
The behaviour of the outputs when an output inhibit is applied can be selected via switches 3 and 4 on bank S4 to suit the process. When the BASP signal is revoked, the outputs assume the state stipulated by the IP 240.



on: Output inhibit (BASP) switches the digital outputs to the inactive state
off: Output inhibit (BASP) does not affect the states of the outputs

Fig. 5-5. Setting the Command Output Inhibit "BASP" on Switchbank S4

5.3 Matching to Encoder Signals

You can connect the following to the IP 240 as **position encoders**:

- symmetrical incremental encoders with 5 V differential signals complying with RS 422A via inputs A/A, B/B, Z/Z
  and
- asymmetrical incremental encoders with 5 V DC or 24 V DC signals via the inputs A*, B* and Z*.

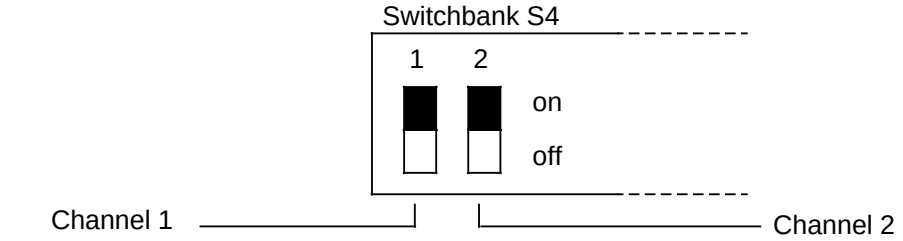
You can connect encoders with 5 V DC or 24 V DC signals to the CLK, GT and IN **binary inputs**.

You can set coding switches for matching the IP 240 to the encoder signals.

5.3.1 Settings for Symmetrical or Asymmetrical Signals

All incremental encoders whose outputs comply with the RS 422 A standard supply symmetrical signals A, B and Z and their inverted signals. These encoders have line drivers at the outputs, e.g. 26LS31, 75172 or 75174.

All incremental encoders whose outputs produce a 5 V/24 V DC level supply asymmetrical signals A*, B* and Z*. These encoders have stages which switch to P potential at the outputs or open collector outputs connected to 5 V/24 V via external pull-up resistors.

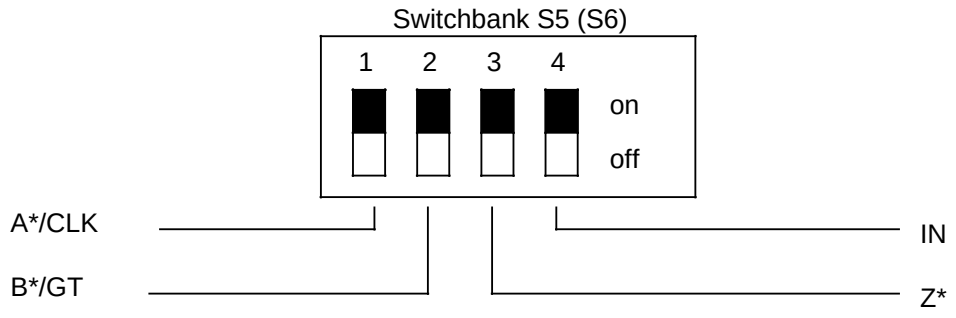


On: Asymmetrical signals A*, B*, Z*
Off: Symmetrical signals A/$\overline{A}$, B/$\overline{B}$, Z/$\overline{Z}$

Fig. 5-6. Setting Switchbank S4 for Symmetrical or Asymmetrical Signals

5.3.2 Settings for Encoder Signal Levels

Input signals A*/CLK, B*/GT, Z* and IN may be adapted to **5 V DC** input level or **24 V DC** input level. The input signals for channel 1 are set on switchbank S5, and for channel 2 on switchbank S6.



On: 24 V DC input level
Off: 5 V DC input level

Fig. 5-7. Setting the Encoder Signal Level on Switchbanks S5 and S6

Figures

Tables

6 Functional Description

6.1 Module Functions

The IP 240 is an intelligent I/O module for acquiring and preprocessing encoder and counting pulses. The module has two channels and can be initialized for the relevant application via the user program.

6.1.1 Modes

The IP 240 can be operated in the positon decoding, counting, positioning and IP 252 expansion modes.
The two channels of the IP 240 module can be initialized separately in the position decoding, positioning and counting modes. In IP 252 expansion mode, both channels are assigned to this mode.

Position decoding
In the position decoding mode, incremental encoder signals are summated to an actual value with the correct sign, and compared cyclically to preset start-of-track and end-of-track values. The sign of the pulses is derived from the phase displacement between encoder signals A and B. A zero offset can be specified for the actual value.
A measuring system can be calibrated to a reference point by means of a reference point approach.

Counting
In counting mode, positve-going signal edges at the counting input are counted in a down counter, under gate control, starting with an initial value. Counting can be enabled by an external gate signal or by a control bit.
Various output reactions can be logically combined when the count reaches zero. After zero, the pulses are acquired with a negative sign when a gate signal is active.

IP 252 expansion (only S5-115U)
In the IP 252 expansion mode, the IP 240 makes both channels available to the IP 252 digital closed-loop control module for the connection of other incremental encoders.
In this mode, the input signals are processed as for positon decoding. Data interchange between the two I/O modules is direct.

Positioning
When the IP 240 is initialized for positioning mode, it can be used for controlled positioning with cutoff points. Up to 254 positions per channel can be stored on the IP for this purpose. Once a position has been selected, the IP itself can control the traversing speed or the direction of travel over the IP outputs. Incremental decoders are used for position sensing.
Three methods of synchronization are possible in this mode. In addition, the actual value can be matched via a zero offset.

6.1.2 Digital Outputs

The digital outputs on the module can be used for direct driving of actuators and displays for particular process states (actual values).
The digital outputs can be set to a predefined state by the user program. This takes place at a higher level than when the outputs are set as a function of the actual value.

Position decoding
For positon decoding, two outputs are available per channel; these can be assigned to tracks when the channels are initialized. If the actual value enters one of these tracks, the corresponding output is energized. The outputs are deenergized when the value exits the track.

Counting
In the counting mode, output D 1 of each channel can be set when the count reaches ”0”.

IP 252 expansion
No digital outputs are available.

Positioning
In positioning mode, two outputs are available per channel. Depending on configuring, the outputs are set for controlling the direction of travel or the speed. The outputs are reset when the specified cutoff points are reached.

6.1.3 Interrupt generation

The IP 240 can relay certain events directly to the S5 CPU by generating an interrupt request. Similarly to setting the outputs, a process interrupt can be made dependent on the actual value.
An interrupt request can also be generated by status signals.

Status signals with interrupt capability
In the position decoding and positioning mode, the following status signals have interrupt capability:
- Overrange
- Error in zero mark monitoring
- Wirebreak/short-circuit in the set encoder lines for encoders with symmetrical signals

In the counting mode, a range violation is an interrupt- capable status signal.
Interrupts cannot be generated in IP 252 expansion mode.

Interrupt request
An interrupt request remains pending until the CPU confirms the request by reading the interrupt request bytes. This usually takes place in the relevant interrupt OB.

6.1.4 LEDs

The module has four green status and three red fault LEDs (Section 2.3).

States of the digital outputs (green LEDs)
Each green LED indicates the state of a digital output. When an output is energized, the corresponding LED lights up.

Wirebreak/short-circuit (red WB LED)
When a channel is set to symmetrical pulses, the encoder cable is monitored by evaluating the two pulse trains of an encoder track. Detection of a wirebreak/short-circuit is indicated separately for each channel for the duration of the fault condition with the red WB (**W**ire**B**reak) LED.

Hardware fault (red MF LED)
The red MF (**M**odule **F**ault) LED indicates a hardware fault on the module. If the LED does not darken within 3 s following power-up, the module has a hardware fault and cannot function properly.

6.2 Programming

The user program selects the modes and controls the IP240.
Configuring and control function blocks are available for this purpose; these handle the data interchange between the S5 CPU and the IP 240 module. The standard function blocks are PLC-specific. All data to be transferred is managed in a data block which must be created by the user.

Table 6-1. Standard Function Blocks

Mode / Functions and data blocks	Positioning	Position decoding	Counting	IP 252 expansion
Configuring function block	FB 167	FB 169	FB 171	FB 173
Control function block	FB 168	FB 170	FB 172	
Data block	DB x	DB x	DB x	DB x

x = Number of the data block (3 to 255)

Any errors occurring during execution of an FB are flagged in an error byte as group error and described in detail in data words.

Note

When using both an IP 240 and a WF 625 with operator panel, the numbers of the standard function blocks for one of these modules must be changed, as the FBs for both modules have the same number.

6.2.1 Configuring Function Blocks

Configuring function blocks serve to select the modes. Each mode is assigned its own function block:
- FB 167 for positioning mode (Section 10.23.2)
- FB 169 for position decoding mode (Section 7.3.1)
- FB 171 for counting mode (Section 8.3.1)
- FB 173 for IP 252 expansion mode (Section 9.3.1)

Configuring FBs are normally called in Restart organization blocks (OB20, OB21, OB22). Because channel configuring increases the module firmware's cycle time requirement, the STEP 5 program must be written so as to ensure that the other channel is in a safe wait state while the configuring FB is executing.
The configuring FBs do not disable the servicing of process interrupts. This must be done by the user program.
Before configuring, the FB checks whether it is compatible with the module firmware.

6.2.2 Control Function Blocks

Control function blocks are available for the position decoding, positioning and counting modes:
- FB 168 for positioning mode (Section 10.23.3)
- FB 170 for position decoding mode (Section 7.3.2)
- FB 172 for counting mode (Section 8.3.2)

Control FBs can be invoked without restriction in the user program when configuring has been completed. By assigning the appropriate parameters to the blocks when they are called, various data areas can be transferred from the data block to the IP 240, or can be written into the DB from it.
In the control FBs, servicing of interrupts is enabled from time to time, The scratch flags and system data areas used must therefore be saved in the interrupt service routines (Technical Specifications for Function Blocks).
Before executing, each control FB checks whether the channel it has addressed has been configured for the relevant mode.
The control function blocks for the S5-135U and S5-155U call the subordinate function OB122. It is therefore necessary to use the following CPUs
- CPU 922 from Version 9 onwards (operating system Version 4)
- CPU 928 from Version 2 onwards (6ES5 928-3VA12)

6.2.3 Data Blocks

The data blocks contain all data for the transfer from and to the IP 240. The number of the relevant data block must be specified in the DBNR (**D**ata **B**lock **N**umbe**R**) parameter when the FB is invoked.
The contents of the data blocks are functionally subdivided into three areas:
- Information made available by the IP 240 (general module information, status flags and actual values),
- Specifications entered when initializing the configuring FB (module address, configuration data),
- Control statements as well as initial and final values which are specified when the DB is created or in the user program cycle.

The required block lengths must be observed.

6.3 Restart Characteristics

6.3.1 Power On

After ”Power on” a test routine is initiated on the IP 240 to verify proper functioning of the module.
If the routine executes without error, the module is in a wait state which allows configuring of the channels.
Any errors detected are stored in data words 8 to 10 of the specified data block when configuring, and are indicated with the red MF LED.

The digital outputs are switched to the inactive state after ”Power on”.

6.3.2 CPU STOP

If the CPU goes from the RUN mode to the STOP mode, the IP 240 continues to run in the configured mode.
After a CPU restart, the channels of the module can be reset to an initial state by reconfiguring, or can continue to be operated in the configured mode.
If the channels are not reconfigured, any pending process interrupt requests must be cancelled by reading the interrupt request bytes.

Note

Power failure
No battery backup is provided in the IP 240. All information is lost in the event of a power failure.
Restart
When using an S5-150U or S5-135U with preliminary setting, any scratch flags and system data areas used in the FBs (Technical Specifications for Function Blocks) must be saved in the restart routine (OB21/OB22).
The standard FBs for the S5-155U are programmed in such a way that this is unnecessary.
Bit 3 in the PAFE byte can be set by the control FB, depending on the point at which the program was interrupted (Section 6.4). The data interchange that was in progress when the restart was initiated must be repeated.

6.4 Fault and Error Flagging

Each time a standard function block is called, a flag byte or output byte must be specified as **PAFE** parameter. Any errors occurring are grouped and flagged in this error identifier byte. For this purpose, the current error state is written into this byte at the end of a function block.
The possible errors subdivided into five categories, and flagged as follows by setting a PAFE byte (Table 6.2). If a more detailed error description is possible, it is entered in KH format in data words 8 to 10 and 13 of the specified data block as error message. The user must himself delete the error messages in the DB.

The PAFE byte should be scanned for zero following every FB call.

Table 6-2. Error Flagging in the PAFE Byte

Bit number PAFE byte	Error category	Exact error description in DB
0	Hardware faults, communication and data errors	DW 8 to 10
1	Parameter and data errors	DW 13
2	Data block number entered is illegal, data block does not exist or is too short, CPU not permissible	-
3	Commencement or continuation of data exchange with the IP 240 was not possible. Delay time for communication with the IP 240 exceeded.	-
7	The function block was aborted prematurely	-

6.4.1 Hardware Faults and Communications Errors

When hardware faults on the IP 240 or communications errors with the IP 240 occur, the function block sets bit 0 in the PAFE byte.

The function block enters the exact causes of the errors in data words 8 to 10 of the specified data block. The **D**ata word **L**eft (DL) contains the error number, the **D**ata word **R**ight (DR) the error extension.
The last three errors to occur are entered. Data word 10 contains the last error to have been detected.
Once they have been read out, communications error flags are reset on the IP 240. Hardware fault flags are not reset and can be read out repeatedly.

Table 6-3. Hardware Fault Codes

Fault code (DW 8 to 10)	Description
1001	Watchdog error
1002	Error in checksum test (EPROM)
1003	Error in counter test (82C54)
101n	Main memory test no. n faulty, n=1 to 8
102n	Transfer buffer test no. n faulty, n=1 to 8

Table 6-4. Communications Error Codes

Error code	Description
4000	Protocol error
41nn	Job number illegal; nn = old job number

6.4.2 Parameter and Data Errors

Parameter errors
When parameter errors occur, the function block sets bit 1 in the PAFE byte.
Parameter errors occur when

- the function block is not compatible with the IP firmware
- the function block is incorrectly initialized
- the channel was not configured, or it was not configured for this control FB.

The function block enters the precise cause of error in data word 13 of the specified data block, and the data block is exited.

Table 6-5. Parameter Error Codes

Error code in DW 13	Description
0001	Module address is illegal
0002	Channel number is illegal
0003	Configuration parameter incorrect
0004	FB not executable with IP firmware
0210	Channel not configured
0211	Control FB not compatible with the configured mode or the specified data block
0212	Function number illegal

Data errors
Data errors occur when the specified data e.g.

- are out of range,
- not in BCD format,
- contain illegal bit combinations.

These errors can be flagged by both the function block and the module firmware.

When the function block detects a data error, it sets bit 1 in the PAFE byte and enters the precise cause of error in data word 13 of the specified data block. The FB is then exited; the function is not executed.

When the module firmware detects a data error, the function block sets bit 0 in the PAFE byte.

The function block reads out the precise cause of error from the IP and enters it in data words 8 to 10 of the specified data block. Once the error has been read out, the IP 240 resets its error flag.

> **Note**
>
> See Chapter 14 for a complete table of error codes.

6.5 Multiprocessor Operation

In the S5-135U and S5-115U PLCs with multiprocessor capability,the IP 240 can also be used when these PLCs are equipped with more than one processor.
Note that an IP 240 can be addressed by **one** processor **only**. The IP 240 must be assigned to the CPU with which it is to interchange data.

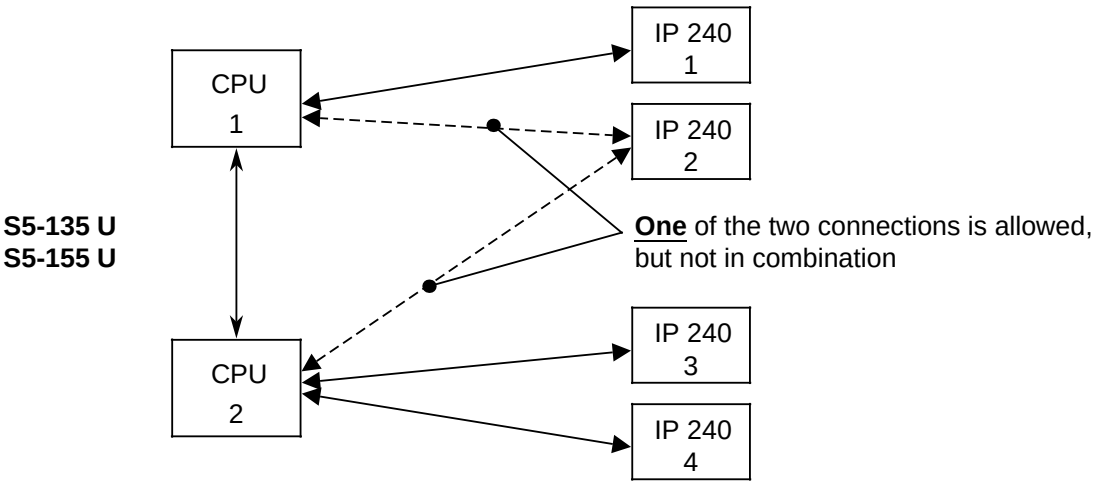


Fig. 6-1. Data Interchange in Programmable Controllers with Multiprocessor Capability

Note

A wait time of 100 ms mut be programmed for the IP 240 in the restart OBs (OB20, 21 and 22) prior to the first function block call.
Failure to do so may result in an abort of the first attempt at data interchange with the IP 240.

Figures

Tables

7 Position Decoding

7.1 Application

In this mode, the IP 240 can be used in all applications in which position changes are to detected and decoded using incremental encoders. The module can process encoder pulse trains with a frequency of up to 500 kHz for symmetrical encoders and 100 kHz for asymmetrical encoders.
The function of a cam controller can be simulated by presetting reference tracks. Error detection during signal acquisition is possible by monitoring signals.

7.2 Principle of Operation

For the position decoding mode the following STEP 5 blocks are necessary:

- A data block
  You must create a data block (DB) prior to calling the configuring function block for the first time. New data must be entered in this DB prior to its transfer to the IP 240 by the FB 170.
  Data that is read from the IP 240 is stored in this DB by control FB 170.
- Configuring FB 169
  You structure one or both channels of the IP 240 in position decoding mode with configuring FB 169. The configuring FB is normally called in the restart OB.
- Control FB 170
  The control FB 170 is called in the cyclic program or the interrupt program. By means of the FB parameter FKT, you can specify whether data is to be read from or transferred to the IP 240.

7.2.1 Actual Value

Formation of the actual value
An internal, signed count is determined by counting the pulses and evaluating the phase displacement between encoder pulse trains A and B. The actual value **IST** is obtained from this count by addition with the definable zero offset **NVER**.

Counting direction
The IP 240's encoder pulse count is

- an up count when the **B signal** is the leading signal.
- a down count when the **A signal** is the leading signal.

In IP 252 expansion mode, a leading A signal corresponds to a positive speed.

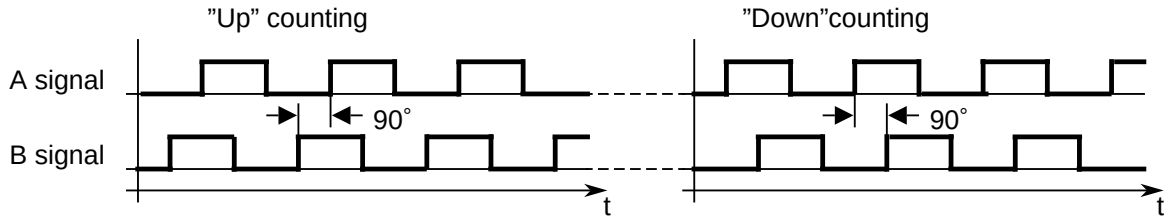


Fig. 7-1. Counting Direction in Positon Decoding Mode

Changing the counting direction
To change the counting direction, you must interchange the encoder signal connections as follows:
- for symmetrical encoders, interchange A/A and B/B.
- for asymmetrical encoders, interchange A* and B*.

Actual value range and overrange
The actual value range is defined as - 99,999 to+99,999.

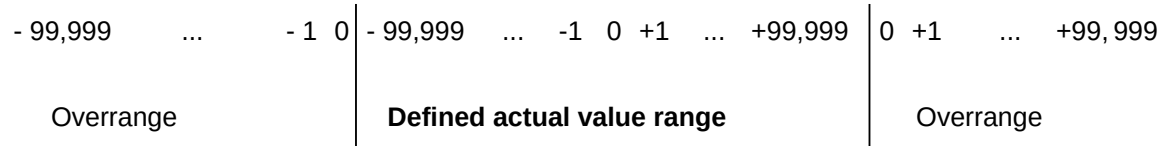


Fig. 7-2. Actual Value and Overrange in Positon Decoding Mode

When the counter leaves the defined actual value range, it enters the overrange and the IP sets the **UEBL** status bit (Overflow). In the overrange, pulse decoding continues as in the defined range. However, the IP no longer compares the actual value with the predefined track limits. The current state of the REFn bits is recorded (REFn bits Section 7.2.3).
Status bit UEBL can be used to trigger an interrupt. You must specify this, if required, in the PRA2 parameter during configuring (Section 7.3.1).

It is reset
- when the status area is read
- when the interrupt request bytes are read if the overrange has triggered the interrupt.

Reading the actual value
The actual value is updated in every module firmware cycle (operating system for the IP 240). To be able to read the current actual value from the DB, you must first call control FB 170 and parameterize function 1 ”Reading the actual value and the status bits” (Section 7.3.2).
The CPU fetches the current data from the IP and writes it to the data block. The data for the actual value is entered as follows:

- DW 30/31 Absolute actual value in BCD code
- DW 32/33 Absolute actual value binary coded
- D 19.0 Sign of the actual value (status bit SG)

After configuring, the value ”0” is specified as actual value.

Zero offset
You can define a zero offset for the IP within the range - 99,999 to +99,999. You must store the zero offset in BCD code in the installed data block in data words 66 and 67 (Section 7.3.3). Now call control FB 170 and parameterize function 5 ”Write zero offset” (Section 7.3.2). The CPU then transfers the data from the DB to the IP.
After transfer of the zero offset, the actual value is modified by the difference between the old and the new zero offset.

$$IST_{new} = IST_{old} + (NVER_{new} - NVER_{old})$$

The zero offset value thus always offsets the zero point of the actual value range to the reference point. A zero offset can be revoked by transferring a ”0” value to the IP. Configuring FB 169 does not transfer the zero offset entered in the DB.
Configuring FB 169 does not transfer the zero offset entered in the DB.

- ”Set actual value” at the software level
  With the following sequence of instructions, you can assign a specific actual value to the current location by transferring two zero offsets:

  write the negated new setpoint actual value as zero offset,
  read the actual value,
  invert the sign of the actual value,
  write this negated actual value as new zero offset,
  read the actual value and compare it with the setpoint actual value.

  This software-based method of setting an actual value may be used only when the actual value does **not** change between ”Read actual value” (step 2) and ”Write new zero offset” (step 4).
  Failure to observe this rule will cause the location of setpoint actual value to vary with the traversing speed and the response time until the new zero offset has been written. An additional zero crossing or actual value overflow would then produce a completely falsified new actual value.

7.2.2 Resolution

Resolution can be increased by configuring a pulse multiplication. To do this, enter the desired resolution in parameter **AFL** in configuring FB 169 (Section 7.3.1).
The precision of the displacement distance decoded can be improved by doubling or quadrupling the resolution. The available traversing range is reduced by factor 2 or 4.

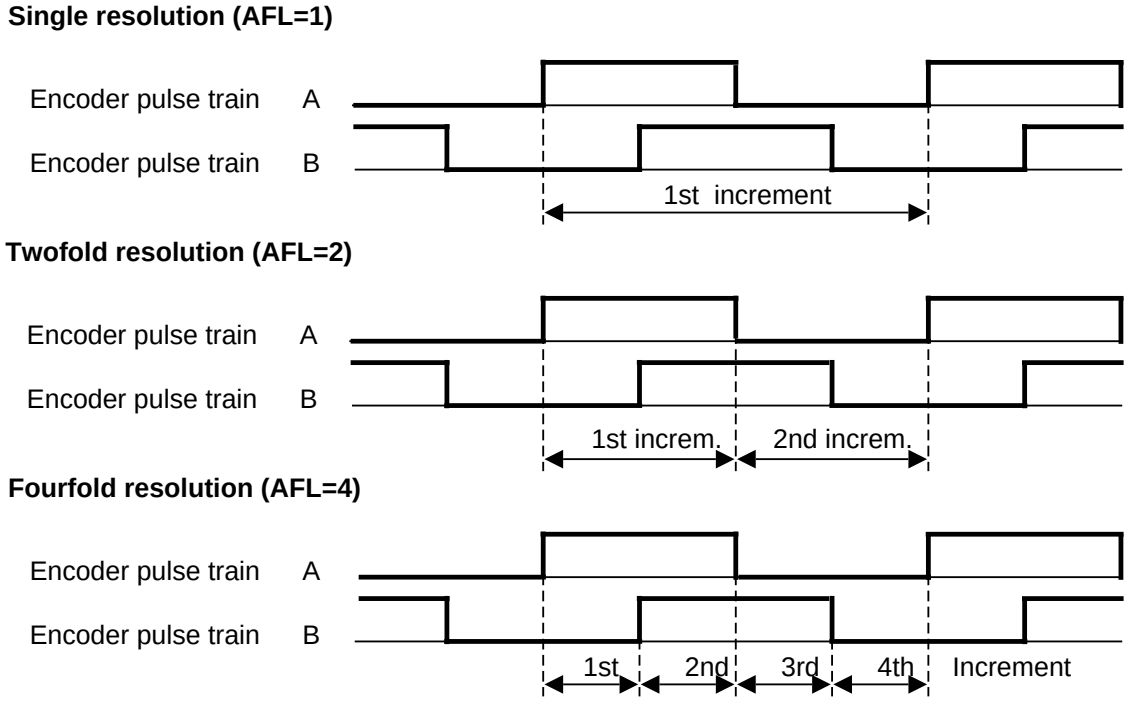


Fig. 7-3. Evaluating the Encoder Pulses

Example:
The position encoder emits 1000 pulses/revolution. The spindle has a gradient of 50 mm/revolution. The position encoder therefore emits 1000 pulses for a distance of 50 mm. The IP 240 processes up to 199,998 increments within the defined actual value range. This results in the following traversing ranges:

Table 7-1. Sample Traversing Ranges

Resolution	Simple	Twofold	Fourfold
Traversing range	9,999.9 mm	4,999.9 mm	2,499.9 mm
Traversing distance/increment	50 µm	25 µm	12.5 µm

7.2.3 Reference Tracks

Up to eight reference tracks can be defined for cam simulation by specifying initial and final values **ANF1** to **ANF8** and **END1** to **END8**. In every module firmware cycle, the limit values are compared with the actual value. If the actual value is within a track (including track limits), a status bit REFn is set.
Identical and overlapping reference tracks are possible. A minimum track width of one increment (ANFn=ENDn) is permissible.

Entering limit values in the data block
Data words DW 34 to 65 are reserved in the data block for the input of limit values. Two data words are provided for every limit value.
The limit values must be entered in BCD code within a range of - 99,999 to+99,999.
The initial value ANFn of a track n must be smaller than or equal to the final value ENDn of track n.
Otherwise the corresponding bit REFn is not set for any actual value.
Tables 7-2 and 7-3 show the data format in which the limit values must be entered, in this case for track 1.

Table 7-2. Initial Value of the First Track (ANF1)

Data word	Bits 7	6	5	4	3	2	1	0
DL 34	0	0	0	0	0	0	0	SG
DR 34	0	0	0	0	10^4			
DL 35	10^3				10^2			
DR 35	10^1				10^0			

SG = 1 the initial value is negative
= 0 the initial value is positive

Table 7-3. Final Value of the First Track (END1)

Data word	Bits 7	6	5	4	3	2	1	0
DL 36	0	0	0	0	0	0	0	SG
DR 36	0	0	0	0	10^4			
DL 37	10^3				10^2			
DR 37	10^1				10^0			

SG = 1 the initial value is negative
= 0 the initial value is positive

Transfer of the initial values from the data block to the IP 240
The limit values are initially transferred to the IP with configuring FB 169.
During operation, you can enter modified limit values with control FB 170.

- Transfer by calling configuring FB 169
  Enter the limit values which are to be transferred to the IP in DR 29. In DR 29, one bit is assigned to each track. (Table 7.4)
- Transfer by calling control FB 170
  Enter the track whose limit values are to be modified in DR 29. Choose only those tracks whose limit values were transferred with configuring FB 169.
  Now call control FB 170 and parameterize function 4 ”Write initial and final track values”.

Table 7-4. Identification of the Tracks to be Transferred

Data word	Bits 7	6	5	4	3	2	1	0
DL 29 DR 29	0 TR8	0 TR7	0 TR6	0 TR5	0 TR4	0 TR3	0 TR2	0 TR1

TRn =1 the track limits for this track are to be transferred to the IP
=0 the track limits for this track are not to be transferred to the IP

Example: You have set bits 2, 4, 5 and 7 in DR 29 on configuration. Limit values for tracks 3, 5, 6 and 8 are transferred to the IP.

1. You now wish to modify the limit values for track 5. Set only bit 4 of DR 29. Now call control FB 170.

2. You wish to use track 7 and transfer the limit values to the IP. You set bit 6 and call control FB 170. In DW 13 you will find error code KH=0207 ”Limit values for track 7 cannot be transferred”.

Monitoring the reference tracks
The actual value is compared with the track limits ANFn and ENDn in every module firmware cycle. If the actual value is within a track (including limits), the status bit (**REF 1** to **REF 8**) assigned to the track is set.
If the initial value exceeds the final value, the corresponding REFn bit is not set for any actual value.

Should a signal decoding error or range violation occur (Section 7.2.6), the status of the REFn bits is frozen. The REFn bits are not updated again until the comparison of the actual value with the track limits is reinitiated
- following a new reference point approach (Section 7.2.9) or
- following transfer of a zero offset.

Triggering a process interrupt
Every REFn bit can trigger a process interrupt when it goes from 0 to 1 (rising edge). You must indicate which REFn bits are to trigger interrupts by setting the corresponding **bits (0 to 7)** in the **PRA1** parameter for configuring FB 169. Each of these bits is allocated to a separate track.
The triggering of interrupts is independent of synchronization of actual-value acquisition.

You may also use **bit 8** of the **PRA1** parameter to indicate the change of actual value after which an interrupt is triggered.
If you set **PRA1/8** to "**1**", a change in the REF bit from 0 to 1 will trigger an interrupt when the actual value
- enters the track over a track limit,
- lies within a track following transfer of a zero offset,
- lies within a track following modification of track limits or
- lies within a track following termination of a reference point approach.

No interrupt is triggered when the actual value lies within a track following configuring.

If you set **PRA1/8** to "**0**", a change in the REF bit from 0 to 1 triggers an interrupt only when the actual value enters the track over a track limit.

Note

If PRA 1/8 is set to "0", actual value-dependent triggering of process interrupts is disabled until the end of the next module firmware cycle in the following cases:
- for all of the channel's tracks following transfer of a zero offset
  and
- for the modified tracks following the transfer of new track limits.

No interrupt is triggered if the actual value enters one of these tracks over a track limit at this point.

Setting the digital outputs
Every REFn bit can set one or both of the channel's digital outputs with the 0 1 change. You must specify this in FB 169 in **bits 0 to 7** of the **DIG1** parameter for output 1 (D1) and **bits 0 to 7** of the **DIG2** parameter for output 2 (D2). Each of these bits is allocated to a track, and each is used to indicate whether the corresponding REFn bit is to set one or both digital outputs.
The outputs are set without regard to sychronization of actual-value acquisition.

Bit 9 of the **DIGn** parameter (n=1 or 2) can be used to define the conditions contingent to setting an output.
If you set **DIGn/9** to "**1**", a change in the REF bit from 0 to 1 sets the output when the actual value
- enters the track over a track limit,
- lies within a track following transfer of a zero offset,
- lies within a track following modification of track limits ,
- lies within a track following termination of a reference point approach or
- lies within a track when the IP 240 enables the outputs (Section 7.2.5).

No output is energized when the actual value lies within a track following configuring.

If you set bit **DIGn/9** to "**0**", a change in the REF bit from 0 to 1 sets the output only when the actual value enters the track over a track limit.

Note

If DIGn/9 is set to "0", actual value-dependent triggering of process interrupts is disabled until the end of the next module firmware cycle in the following cases:

- for all of the channel's tracks following transfer of a zero offset
  and
- for the modified tracks following the transfer of new track limits.

No output is switched on if the actual value enters one of these tracks over a track limit at this point.

Resetting the digital outputs

After they have been set, the digital outputs can be reset:

- by the S5 CPU by setting control bits
- by the IP 240 in dependence on the actual value when the track is exited.

You can specify the IP's reaction to the exiting of a track for each output separately over **bit 8** of the **DIGn** parameter (n=1 or 2).

If you set **DIGn/8** to "1", the IP 240 automatically resets the digital outputs

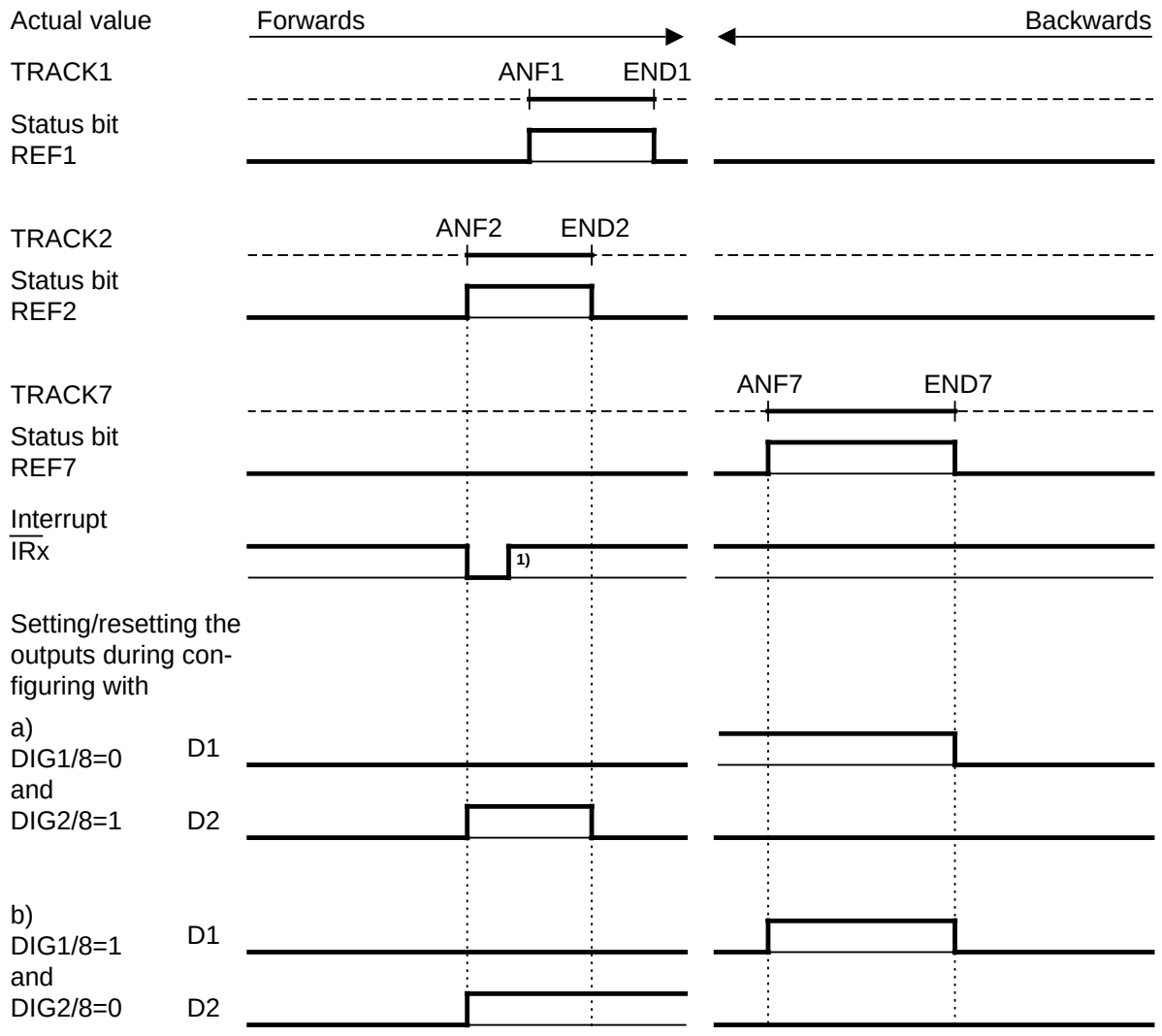
- when the actual value once again exited the track and does not lie within any other track allocated to this output.
  It makes no difference whether the actual value exited the track over a track limit, because of a zero offset, or due to modification of the track limits.
- when the IP detected a signal acquisition error or range violation.
- when transfer of the REF control bit initiates a new reference point approach.
- when the S5 CPU enables actual value-dependent switching of the output by the IP and the actual value does not lie within a track.

If you set **DIGn/8** to "0", the IP 240 does not automatically reset the output.
You can reset the output only by setting control bits DAnF and DAnS in DL17 to "0" and then transferring the control bits to the IP with control FB 170.

Figure 7-4 shows an example of actual-value dependent setting and resetting of digital outputs.

Note

For the IP 240 to set and reset the digital outputs on the basis of the actual value, you must enable the outputs over control bits DAnF and DAnS (n=1 or 2).
To do so, set control bit DAnF to "0" and DAnS to "1" in DL17, then transfer the control bits to the IP 240 by invoking control FB 170 and initializing it for function 2 "Write control bits".



1) The interrupt request is reset when the interrupt request bytes are scanned.

Fig. 7-4. Evaluating the Reference Tracks

Explanations:

- An interrupt is to be triggered as soon as the actual value enters TRACK 2
- Output D2 has been coupled to TRACK 2 and output D1 to TRACK 7.

Triggering the interrupt
Interrupt IRx is generated as soon as the actual value enters TRACK 2.

Setting/resetting the outputs:

To a) Digital output D2 is set when the TRACK 2 is entered and reset when it is exited.
Digital output D1 is set when TRACK 7 is entered, and must be reset by setting control bit DA1F to 0 and DA1S to 0.

To b) Digital output D2 is set when TRACK 2 is entered, and must be reset by setting control bits DA2F to 0 and DA2S to 0.
Digital output D1 is set when TRACK 7 is entered and reset when it is exited.

If an output is coupled to several overlapping tracks, these tracks are treated as a single track as regards actual value-dependent setting and resetting of the output.

Traversing speed and track width
In order for entry into a track to be detectable in every module firmware cycle, the traversing speed must be matched to the minimum track width.
The encoder pulses acquired by the IP are counted in a counter chip. The current (internal) count is read out once in each module firmware cycle and then postprocessed to produce the (external) actual value. The track limits are compared to this actual value. To ensure unambiguous detection track entry, a track must not be entered and then exited in the interval between two count readouts (t_{LZ}). Because the firmware cycle is asynchronous (free-running), t_{LZ} is dependent on the firmware on-load.

The maximum interval between two readouts from the counter chip is computed as follows:

$t_{LZ\ max.} = t_{ka1\ max.} + t_{ka2\ max.} + 2 \cdot t_{kom\ max.}$

where
$t_{ka1\ max.}$ = maximum processing time for channel 1
$t_{ka2\ max.}$ = maximum processing time for channel 2
$t_{kom\ max.}$ = maximum processing time for a data interchange

In Chapter 12 ”Response Times” you will find a list of processing times which will help you compute the minimum track width for your application. In the worst case, i.e. maximum times for channel 1, channel 2 and data interchange, $t_{LZ\ max.}$ computes to 7.5 ms.

7.2.4 Hysteresis

Mechanical disturbances can cause minor changes in the actual value. A fluctuation of the actual value around a track limit can cause continuous triggering of interrupts and setting and resetting of outputs. To avoid this, an adjustable hysteresis allows another interrupt to be generated or an output to be set or reset again only when the actual value has moved away from the track limit by at least the value defined by the hyteresis. This, in turn, allows the actual value to oscillate in the range defined by track limit ± hysteresis without triggering an interrupt or affecting an output.

A hyteresis value>0 increases the module firmware's cyle time in dependence on the number of tracks used (Chapter 12).

Note

The hysteresis does not affect setting or resetting of the REF bits.

Defining the hysteresis
The hysteresis can be preset in BCD in the data block in data byte DR 22 (Section 7.3.3) in the range 0 to 99. It applies to all tracks of a channel and is only transferred to the IP 240 during a configuring pass.

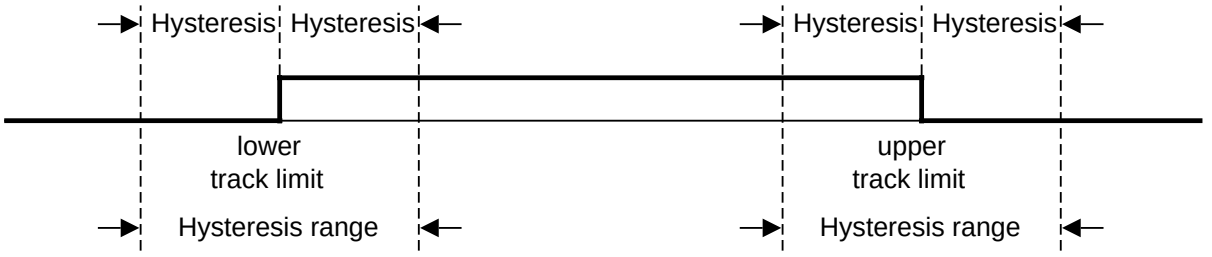


Fig. 7-5. Track with Hysteresis

In order to prevent the hysteresis from encompassing, the entire track value defined for the hysteresis should be smaller than the minimum track width.

Influence of the hysteresis on interrupt generation
Interrupts are always generated when an assigned track is reached. Following generation of an interrupt, the actual value must have exited the hysteresis range for the relevant track limit before entry into a new track can generate an interrupt.
If the hysteresis for the original track is still in force when a new track is entered, no interrupt is generated upon entry into the new track.

Influence of the hyteresis on the outputs
A hysteresis affects the outputs only when
- the channel was configured with DIGn/8=1
  (the IP 240 is to reset the outputs when the track is exited) and
- the outputs were enabled for setting and resetting by the IP
  (Control bit DAnF=0 and control bit DAnS=1 were transferred to the IP).

If a track is traversed without a reversal of the direction of travel, the associated output is set at the first track limit and reset at the second track limit (Fig. 7-6). This is also the case when the second track limit lies within the hysteresis range of the first track limit.

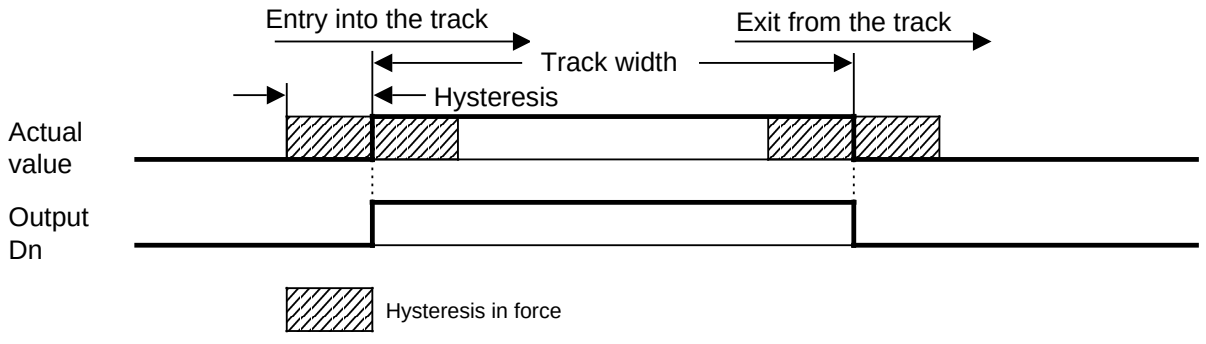


Fig. 7-6. Switching an Output on Traversing a Track

If the direction is reversed outside the hysteresis range following switching of an output, the switching point at the track limit is retained (Fig. 7-7).

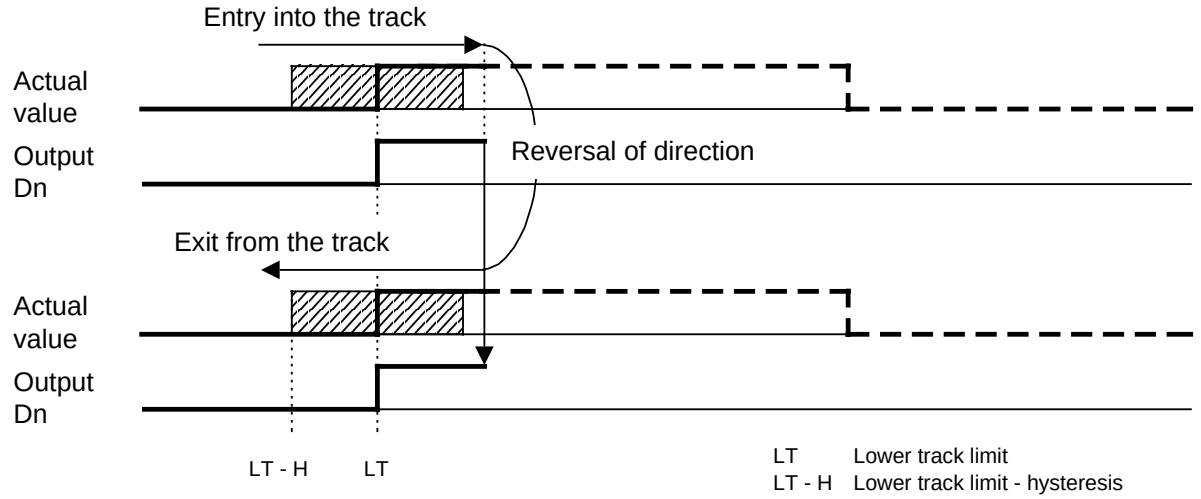


Fig. 7-7. Resetting of an Output Following a Reversal of Direction Outside the Hysteresis Range

If the direction is reversed within the hysteresis range following switching of an output, the hysteresis offsets the switching point by the value of the hysteresis.

a) Resetting of an output
Fig. 7-8 shows how an output is switched upon entry and upon exiting of the lower track limit. The output is set when the lower track limit is exceeded, and the specified hysteresis value goes into force for this limit. The direction is reversed within the range of the hysteresis. The output is reset when the actual value reaches the ”lower track limit - hysteresis”.

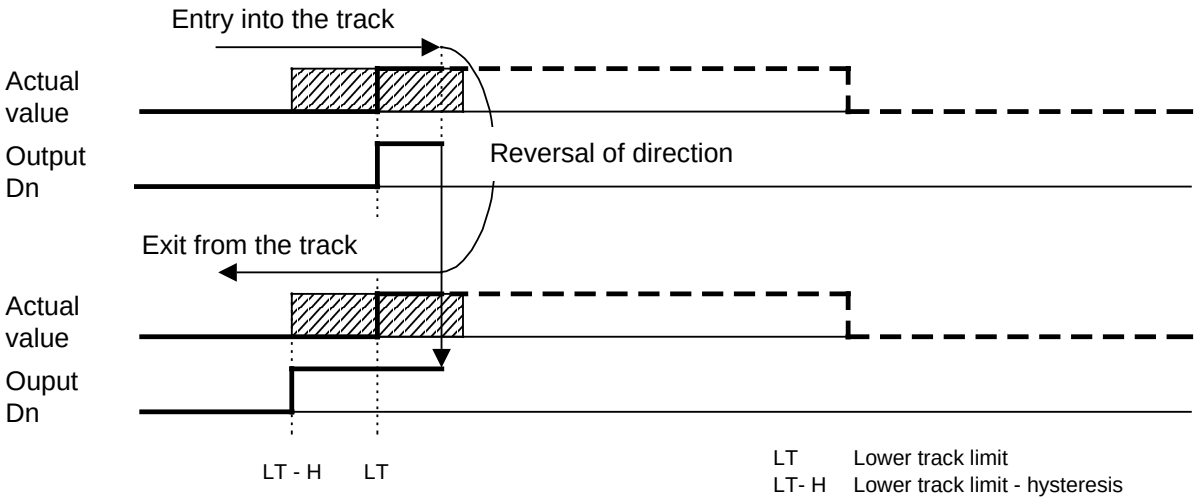


Fig. 7-8. Resetting an Output Following a Reversal of Direction Within the Hysteresis Range

The output is switched analogously upon entry into and upon exit from the upper track limit. The output is reset when the actual value reaches the ”upper track limit+hysteresis”.
(without Fig.)

b) Setting of an output
Fig. 7-9 shows switching of an output upon exit from and upon entry into the upper track limit.
The output is reset when the upper track limit is exceeded, and the specified hysteresis value goes into force for this limit. The direction is reversed within the hysteresis range. The output is set when the actual value reaches the ”upper track limit - hysteresis”.

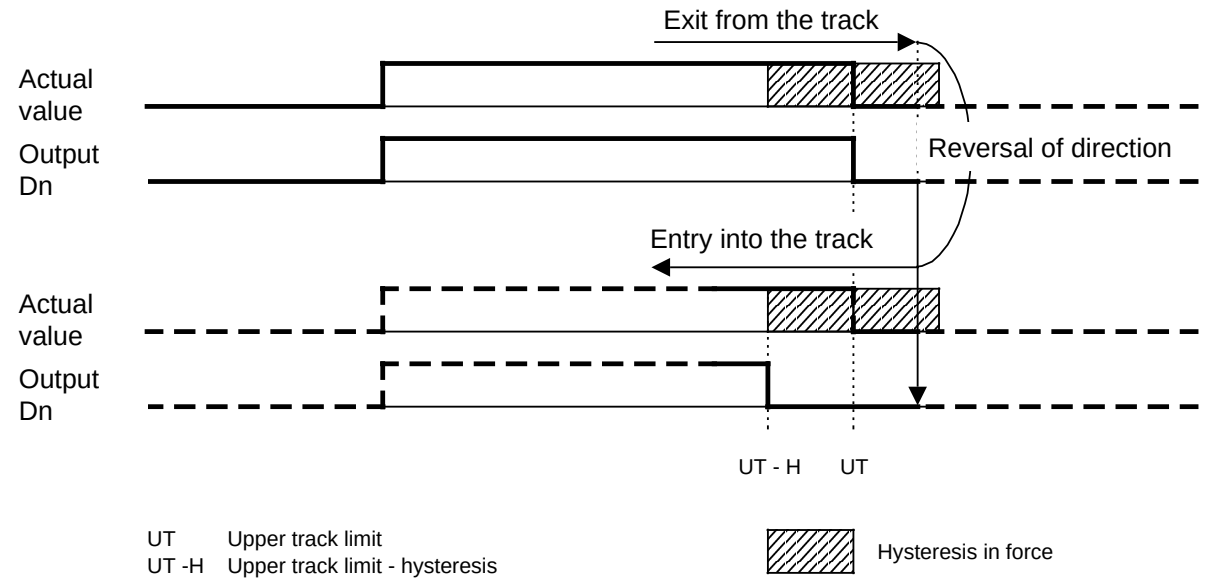


Fig. 7-9. Setting an Output Following a Reversal of Direction Within the Hysteresis Range

The output is switched analogously upon exit from and upon entry into the lower track limit. The output is set when the actual value reaches the ”lower track limit+hysteresis”.
(without Fig.)

If an output was allocated during the configuring phase to several overlapping tracks, a hysteresis is taken into account only on the lower track limit of the lowest and on the upper track limit of the highest track.

7.2.5 Forcing the IP Outputs

You can use control bits **DAnF** and **DAnS** (n=1 for digital output 1 or n=2 for digital output 2) to indicate whether output D1 or D2

- is to be enabled for actual value-dependent switching by the IP
  (if so, set DAnF to 0 and DAnS to 1 in DL17)
- is to be set without regard to the actual value
  (if so, set DAnF to 1 and DAnS to 1 in DL17)
- is to be reset without regard to the actual value
  (if so, set DAnF to 0 and DAnS to 0 in DL17).

After modifying control bits DAnF and DAnS in the DB, you must invoke control FB 170 and initialize it for function 2 ”Write control bits”. The FB then transfers the control bits to the IP.

Status bits **DA1** and **DA2** reflect the current state of the outputs.

7.2.6 Monitoring of Signal Acquisition

Status bit **DRBR** (wirebreak) is set when a wirebreak or short-circuit is detected on the lines for encoders with symmetrical signals. This bit remains set on the IP until the problem has been rectified.

Status bit **NPUE** (zero point monitoring) is set when the IP detects that the number of encoder pulses between two zero marks (Z signal) is not divisible by 4 or 5 without a remainder. This method of zero mark monitoring makes it possible to detect spurious or missing pulses. Zero mark monitoring is initiated on the IP 240 only when a reference point approach was terminated with synchronization.
Zero mark monitoring is possible only when the timing of the encoder signals conforms to the specifications discussed in Chapter 13 ”Encoder Signals”. In addition, when you configure the channel you must specify whether the number of pulses between two Z signals is divisible by 4 or by 5 (without a remainder). The **IMP** parameter in configuration FB 169 is provided for this purpose.

The evaluation of zero mark monitoring must be disabled if the required encoder timing conventions are not observed or if the number of encoder pulses between two Z signals is divisible by neither 4 or 5.

The IMP parameter may be initialized to the following values:

IMP = 0 No evaluation of zero mark monitoring.

IMP = 10 The number of encoder pulses between two Z signals is divisible by 5 without a remainder.

IMP = 16 The number of encoder pulses between two Z signals is divisible by 4 without a remainder.

The module firmware scans for wirebreak and zero mark monitoring in every cycle. If a fault is detected,

- the DRBR or NPUE bit is set on the IP,
- the comparison of actual value with track limits is suspended, and
- the SYNC bit (Section 7.2.9) is reset.

In addition, the following are carried out on the basis of the specified configuring data:
- any outputs that are set are reset
- an interrupt is generated for DRBR or NPUE and interrupt bit **DRB** or **NPU** is set in the interrupt request bytes.

Status bit DRBR is reset on the IP when the fault has been rectified and
- the status area has been read at least once or
- the interrupt request bytes were read (Section 7.2.7) and the fault that triggered the interrupt was a wirebreak.

Status bit NPUE is reset on the IP
- following reading of the status area or
- when the interrupt request bytes were read and the fault that triggered the interrupt was a zero mark monitoring problem.

7.2.7 Interrupt Generation and Processing

Status bits REF 1 to REF 8, UEBL, DRBR and NPUE can trigger an interrupt, and are stored as RF 1 to RF 8, UEB, DRB and NPU in interrupt request bytes (Section 7.3.3) on the IP when they show a ”1” value.

Reading the interrupt request bytes
When it detects an interrupt, the CPU invokes an interrupt service OB. In this organization block, you must invoke a control FB and initialize it for function 3 ”Read interrupt request bytes”. The control FB transfers the interrupt request bytes for both channels to data words DW 20 and DW 21 in the specified data block. You can react to the cause of the interrupt by evaluating these bytes.

When these bytes are read,
- the bits in the interrupt request bytes on the IP are reset
- the IP revokes the interrupt request
- status bit UEBL or NPUE is reset when one of these errors caused the interrupt and
- status bit DRBR is reset when the error was rectified and a wirebreak signal was the reason for the interrupt.

Only the DB specified in the relevant control FB parameter can be updated directly, as the interrupt request bytes are read without regard to a specific channel and the current status can be read out from the IP on a one-shot basis only.

> **Note**
>
> Status bits UEBL and NPUE, as well as all interrupt bits in the interrupt request bytes, are reset on the IP 240 once they have been scanned and can therefore be read out on a one-shot basis only.

Masking interrupts
You can mask all bits with interrupt capability in the relevant channel by setting the **AMSK** control bit (D 17.15) and then transferring the control bits to the IP. Masked interrupts do not generate interrupt requests, and are not stored in the interrupt request byte, i.e. they are lost.
No interrupt is generated when the actual value lies within a track with interrupt capability at the instant at which interrupt masking is revoked.

Invoking the interrupt servicing OBs in the S5-150U and S5-155U PLCs (150 mode)
In the S5-150U and S5-155U (150 mode), the associated interrupt servicing OB is invoked at the next block boundary when one of the bits in I/O byte 0 changes its values. Use the **ABIT** parameter in configuring FB 169 to specify whether the OB is to be invoked every time the bit changes its value or only when it goes from 0 to 1.

ABIT parameter
ABIT : KY x,y

- x>0 : Invoke OB on every signal change
- x=0, y=0 to 7 : Invoke OB only on a signal change from 0 to 1.
  In place of y you must enter the number of the bit in PY 0 which you set on switchbank S1 (Section 5.1.2).

7.2.8 Track Comparison Following Configuring and in the Event of an Error

Following configuring, the actual value is set to ”0” and the encoder pulses are counted without further synchronization. The computed actual value is compared to the specified track limits and, depending on the actual value, reference bits are set, interrupts generated, and outputs set.
To prevent the generation of interrupts, you can mask all interrupts for the channel by transferring AMSK=1 or terminate the interrupt service routine after reading out the interrupt request bytes.
You can enable setting of the outputs via the reference bits with control bits DAnF and DAnS.

Errors following transfer of a zero offset
Should a signal acquisition error (DRBR signal) or overrange error occur following configuring or following transfer of a zero offset, the comparison of the updated actual value with the track limits is aborted and the current status of the reference bits frozen.
A subsequent transfer of a zero offset reinitiates the track comparison, and the reference bits are updated. The outputs are set in dependence on the actual value.
Following an overrange error, transfer of a zero offer is equivalent to returning the actual value from overrange to normal range.

Error following a reference point approach
After configuring, the measuring system can be synchronized to a reference point via reference point approach (Section 7.2.9).
If a signal acquisition error or overrange error occurs following synchronization (DRBR or NPUE signal), the comparison of the actual value to the reference tracks is aborted and the reference bits are frozen. The comparison and setting of the outputs can be reenabled via a new reference point approach or by transferring a zero offset.

Following a DRBR error, the next zero mark pulse may also produce an NPUE error, even when a new reference point approach was initiated.

7.2.9 Reference Point Approach

Since incremental encoders cannot indicate the absolute position after a power failure, a reference point must be approached to calibrate a measuring system. The location of the reference point is determined by the zero mark or reference signal (Z signal) emitted by the encoder during a preliminary signal. To generate the preliminary signal, you must connect a bounce-free switching element within the traversing range.
If a zero offset was forwarded to the IP prior to synchronization, the actual value is set to this value at the reference point. The zero point of the actual value range can thus be offset to the reference point. If no zero offset was forwarded to the IP, the actual value is set to ”0”.
A complete reference point approach is not absolutely necessary for position decoding.

Preparations for a reference point approach

Connect the position encoder to the IP 240 (Chapter 4)
Connect the preliminary signal contact to binary input IN.

Reference point approach

Set control bit **REFF** to ”1” (D 17.0)
Forward the control bits to the IP 240 with control FB 170, function 2 (”Write control bits”).
The channel is now in reference point approach mode. No track comparison is made in this mode. If the channel was configured with DIGn/8=1 (the IP is to reset outputs when a track is exited), the active outputs are reset.

- When a ”1” signal is present at preliminary contact input **IN**, the next Z signal from the encoder synchronizes the actual value.
  The preliminary contact signal must be present for at least $t_1$max.=5 ms (Fig. 7-10) prior to the Z signal used for synchronization.
  If the duration of the preliminary contact extends over two or more zero marks, synchronization takes place with every Z signal.
- When a negative-going edge is detected at the preliminary contact input, the **SYNC** bit is set after a delay of $t_2$max.=5 ms, the reference point approach is exited, and the track comparison is initiated.
  Set control bit REFF to ”0”.
  Should you fail to do, so a new referece point approach would be started and the SYNC bit is transferred. The reference point approach may be initiated only once.

Status bit SYNC

The **SYNC** bit is set when the reference point approach was correctly terminated with the synchronization of the actual value.

SYNC is reset

- when a new reference point approach is enabled or
- when an error was detected during position decoding.

> **Note**
>
> Once REFF=1 has been forwarded, the control bits must not be modified until synchronization has been completed unless you want to abort the reference point approach.

Aborting a reference point approach
The reference point approach initiated by setting the REFF bit is normaly terminated, following synchronization, with a negative-going edge at the preliminary contact input.

If, despite this, it is still necessary to exit a reference point approach, this can be done by resetting the REFF bit:

- If the REFF bit is set to ”0” and forwarded to the IP before the positive-going edge is present at the preliminary contact input, the reference point approach is aborted immediately and actual value acquisition with track comparison initiated.
- If the REFF bit is set to ”0” and forwarded to the IP after the positive-going edge was already present at the preliminary contact input, the reference point approach is not aborted until the preliminary contact input shows a negative-going edge. If a valid condition for synchronization occurs in the interim, the actual value is synchronized and the SYNC bit set.

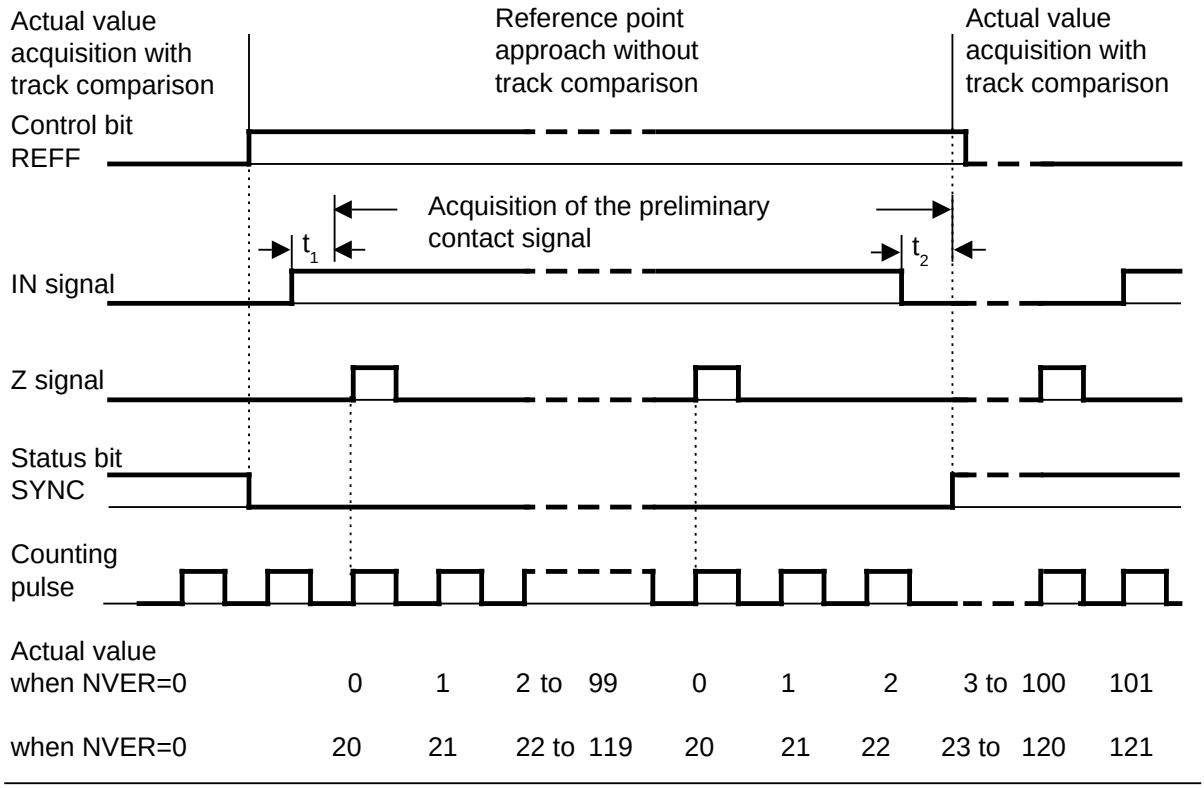


Fig. 7-10. Sequence Diagram for Reference Point Approach

Note

By selecting the traverse speed during the reference point approach and justifying the negative-going initiating contact edge between two zero marks, you must make sure that synchronization always takes place at the same zero mark position.
During reference point approach, the Z signal is evaluated when A=1 and B=1. For information and conventions relating to the location and to the timing of the Z signal and to acquisition of the preliminary contact signal, see Chapter 13 ”Encoder Signals”.
Synchronization is possible in both traversing directions.

7.3 Initializing Standard Function Blocks and Data Block Assignments

7.3.1 Configuring Function Block

FB 169 (STRU.WEG) Configuring data and parameter for operation of the IP 240 in the position decoding mode

Functional description

The configuring function block initially checks the parameter assignments and then transfers the general module data (machine-readable product code of the module, firmware and hardware version) from the IP to the specified data block. It then verifies its compatibility firmware version and transfers the error messages of the initial start check (Section 6.3) to the data block.

The configuring data (parameter entries into FB 169) and the following data areas are then transferred from the DB to the IP 240:

- Initial and final track values
- Hysteresis

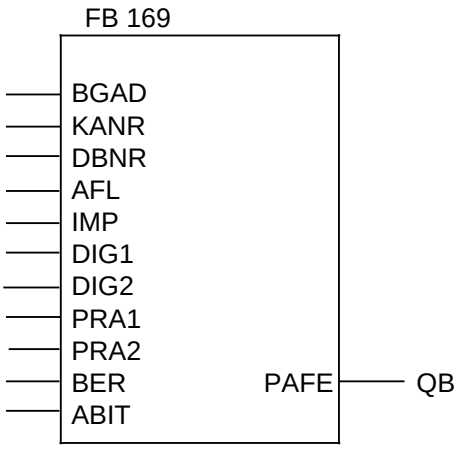
Once the specified channel has been configured without errors, the identifier for the configured mode is entered in DW 23.

If the IP 240 is reconfigured, active outputs and any pending interrupts for the channel are reset.

Hardware faults, communications errors and parameter assignment errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. In the event of an error or fault, the channel is not configured.

Function Block Call

The configuring FB is usually called in the restart organization blocks.

STL	LAD/CFS
: SPA FB 169 NAME : STRU. WEG BGAD : KF KANR : KF DBNR : KF AFL : KF IMP : KF DIG1 : KM DIG2 : KM PRA1 : KM PRA2 : KM PAFE : QB BER : KF ABIT : KY	

Note

Specification of the address space (BER) is dispensed with in the case of the function block for the S5-115U programmable controller (normal P area only, Chapter 3).
Parameter ABIT is not required for the function blocks for the S5-115U and S5-135U.

Table 7-5. Parameters for Configuring FB 169

Name	Parameter type	Data type	Description
BGAD	D	KF	Module starting address
KANR	D	KF	Channel number
DBNR	D	KF	Data block number
AFL	D	KF	Resolution of encoder pulses
IMP	D	KF	Zero mark monitoring
DIG1	D	KM	Assignment of digital output D1 to reference tracks 1 to 8
DIG2	D	KM	Assignment of digital output D2 to reference tracks 1 to 8
PRA1	D	KM	Assignment of a process interrupt to reference tracks 1 to 8
PRA2	D	KM	Assignment of a process interrupt to bits in the status area
PAFE	A	BY	Error identifier byte
BER *	D	KF	Address range (I/O area and extended I/O area)
ABIT **	D	KY	Evaluation of the signal transition for interrupt processing with PY 0 Interrupt bit reserved in I/O byte 0.

* not required for FB 169 for the S5-115U

** not required for FB 169 for the S5-115U and S5-135U

Parameter assignments

BGAD: KF	128 to 240	Starting address of module in P area, divisible by 16
	0 to 240	Starting address of module in Q area, divisible by 16
KANR: KF	1	Channel 1
	2	Channel 2
DBNR: KF	3 to 255	Number of the data block created
AFL : KF	1	Single resolution
	2	Twofold resolution, corresponds to doubling of encoder pulses
	4	Fourfold resolution, corresponds to quadrupling of encoder pulses
IMP : KF	0	No zero mark monitoring
	10	Number of pulses between two zero marks divisible by 5 (without remainder)
	16	Number of pulses between two zero marks divisible by 4 (without remainder)

DIG1 : KM 0000 0000 **Bit 0 to Bit 7**:
0000 0000 Assignment of digital output D1 to reference tracks 1 to 8
\- Bit n = 1 Output D1 is set with assigned reference bit
0000 0011
1111 1111 Bit n = 0 Output D1 is not set with assigned reference bit

Bit 0 : Assignment of track 1 to output D1
Bit 1 : Assignment of track 2 to output D1
: : :
Bit 7 : Assignment of track 8 to output D1

Bit 8 = 0 D1 is not reset when track is exited
= 1 D1 is reset when track is exited

Bit 9 = 0 D1 is set only when track is entered over track limit
= 1 D1 is set when reference bit is ”1”
(except the following channel configuring)

DIG2 : KM 0000 0000 **Bit 0 to Bit 7**:
0000 0000 Assignment of digital output D2 to reference tracks 1 to 8
\- Bit n = 1 Output D2 is set with assigned reference bit
0000 0011
1111 1111 Bit n = 0 Output D2 is not set with assigned reference bit

Bit 0 : Assignment of track 1 to output D2
Bit 1 : Assignment of track 2 to output D2
: : :
Bit 7 : Assignment of track 8 to output D2

Bit 8 = 0 D2 is not reset when track is exited
= 1 D2 is reset when track is exited

Bit 9 = 0 D2 is set only when track is entered over track limit
= 1 D2 is set when reference bit is ”1”
(except following channel configuring)

PRA1 : KM 0000 0000 **Bit 0 to Bit 7**:
0000 0000 Assignment of a process interrupt to reference tracks 1 to 8
\- Bit n= 1 A process interrupt is triggered with an assigned reference bit
0000 0001
1111 1111 Bit n= 0 No process interrupt is triggered with an assigned reference bit

Bit 0 : Assignment of track 1 to a process interrupt
Bit 1 : Assignment of track 2 to a process interrupt
: : :
Bit 7 : Assignment of track 8 to a process interrupt

Bit 8 = 0 An interrupt is generated only when a track is entered over a track limit
= 1 An interrupt is generated when reference bit is ”1”
(except following channel configuring)

PRA2 : KM	0000 0000	Assignment of a process interrupt to bits in the status area	
	0000 0000	Bit n= 1	A process interrupt is generated when status bit is ”1”
	-	Bit n= 0	No process interrupt is generated when status bit is ”1”
	0000 0000		
	0000 0111	**Bit 0** :	Assignment of a counting range violation to a process interrupt
		Bit 1 :	Assignment of a zero mark error to a process interrupt
		Bit 2 :	Assignment of a wirebreak/short-circuit in the encoder lines to a process interrupt
PAFE : QB		Flag byte or output byte (0 to 239) for flagging errors (Section 6.4)	
BER : KF	0	Addressing in the I/O area (P area)	
	1	Addressing in the extended I/O area (Q area)	
ABIT : KY x, y	**x**=0 to 255	x>0 :	Branch to the interrupt OB on every signal transition of the interrupt bit.
		x=0 :	Branch to the interrupt OB only on a 0 to 1 signal transition of the interrupt bit
	y=0 to 7	Interrupt bit reserved in I/O byte 0 as set on switchbank S1	

Note

Process interrupts are not disabled in the configuring function blocks. When using an S5-115U, S5-135U (when set for interrupt servicing at block boundaries) or S5-155U (155U mode), you must write your STEP 5 program so that the configuring FBs cannot be interrupted. Process interrupts are disabled in all restart OBs.

Increase in cycle time due to configuring.
Because channel configuring increases the module firmware's cycle time, you must write your STEP 5 program so that the other channel is in a safe wait state while the configuring FB is executing.

Technical Specifications

Block number : 169

Block name : STRU. WEG

PLC	Library number	Call length/ Block length	CPU	Processing time[1]
S5-115U	P71200-S 5169-D-2	12 words/ 1098 words	941-7UA...	approx. 350 ms
			942-7UA...	approx. 150 ms
			943-7UA...	approx. 85 ms
			944-7UA...	approx. 20 ms
			941-7UB...	approx. 76 ms
			942-7UB...	
			943-7UB...	
			944-7UB...	approx. 20 ms
S5-135U/ S5-155U	P71200-S 9169-D-2	13 words/ 1654 words	922 from A9	approx. 83 ms
			928-3UA...	approx. 56 ms
			928-3UB...	approx. 20 ms
S5-150U	P71200-S 4169-D-1	14 words/ 1660 words		approx. 24 ms
S5-155U	P71200-S 6169-B-1	14 words/ 164 6words	946-3UA.../ 947-3UA...	approx. 23 ms

Nesting depth : 0

Subordinate blocks : none

Assignments in data area : data block specified with DBNR parameter up to and including DW 67

Assignments in flag area : MB 240 to 255

System statements : yes

[1] The processing times indicated apply only to an FB call after a firmware cycle of the IP 240 without data exchange.

7.3.2 Control Function Block

FB 170 (STEU.WEG) Control function block for position decoding mode.

Functional description
The control function block first verifies whether the addressed channel has been configured for the ”position decoding” mode. In accordance with the parameter assignments of the function block, certain data areas are then transferred from the data block to the IP 240 or updated in the DB by reading them from the IP 240.

The following functions are possible:
- Reading the actual value and the status bits
- Writing the control statements (control bits)
- Reading the interrupt request bytes
- Writing the initial and final track values
- Writing the zero offset

Communications and parameter errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. The specified function is not executed in the event of an error.

Function block call
The control FB is usually called in the cyclic program part and in the interrupt organization blocks.

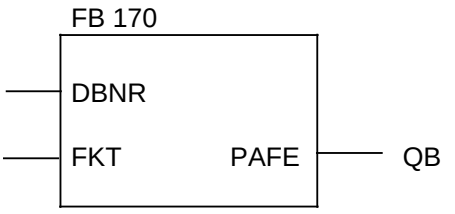
STL	LAD/CFS
: SPA FB 170 NAME: STEU.WEG DBNR : KF FKT : KF PAFE : QB	

Table 7-6. Parameters for Control FB 170

Name	Parameter type	Data type	Description
DBNR	D	KF	Data block number
FKT	D	KF	Function number
PAFE	Q	BY	Error identifier byte

Parameter assignments

DBNR	:	KF	3 to 255	Number of the data block created
FKT	:	KF	1	Read actual value and status bits
			2	Write control statements (control bits)
			3	Read interrupt request bytes
			4	Write initial and final track values
			5	Write zero offset
PAFE	:	QB		Flag byte or output byte in which errors are to be flagged (Section 6.4).

Note

Scratch flags and system data areas are used in the standard function blocks for the purpose of data interchange with the IP 240 (Technical Specifications for the FBs).
You must therefore

- save these flags and data areas at the beginning of the service routines for the S5-115U, S5-135U (when set for interrupt servicing at block boundaries) and S5-115U (155U mode) and reload them at the end of these routines.
- save these flags and data areas at the beginning of the restart (OB21/OB22) of the S5-135U (with basic setting for the restart mode) and reload them at the end of these routines.

Technical Specifications

Block number : 170
Block name : STEU. WEG

PLC	Library number	Call length/ Block length	CPU	Processing time[1] Function	1	2	3	4	5
S5-115U	P71200-S 5170-D-2	5 words/ 975 words	941-7UA...	approx.	38	18	25	80 to 270	28 ms
			942-7UA...	approx.	20	11	14	30 to 112	15 ms
			943-7UA...	approx.	14	6.4	8.2	14 to 65	8.2 ms
			944-7UA...	approx.	3.8	3.3	3.5	5.0 to 18	2.6 ms
			941-7UB... / 942-7UB... / 943-7UB...	approx.	10.5	6	7.2	11 to 54	7.8 ms
			944-7UB...	approx.	3.8	3.3	3.5	1.9 to 17	2.2 ms
S5-135U/ S5-155U	P71200-S 9170-D-2	5 words/ 1539 words	922 ab A9	approx.	10	6.6	8.4	19 to 68	9.0 ms
			928-3UA...	approx.	5.8	3.5	4.4	11 to 45	4.8 ms
			928-3UB...	approx.	3.1	3.3	3.2	1.7 to 4.0	3.9 ms
S5-150U	P71200-S 4170-D-1	5 words/ 1508 words		approx.	1.7	1.2	1.4	3.4 to 18	1.5 ms
S5-155U	P71200-S 6170-B-1	5 words/ 1650 words	946-3UA.../ 947-3UA...	approx.	4.3	3.8	4.2	2.7 to 17	2.1 to 3.7 ms

Nesting depth : 0
Subordinate blocks : S5-115U OB160 (only CPUs ...-7UB...)
S5-135U OB122
S5-155U OB91, OB122
Assignments in data area : data block specified with DBNR parameter up to and including DW 67
Assignments in flag area : MB 240 to 255
System statements : yes

[1] The specified processing times are for an FB call following an IP 240 firmware cycle without data interchange. Note that

- when data have been read from the IP 240, further data interchange in the same firmware cycle is disabled.
- when new data have been written to the IP 240, further data interchange in the same and in the next cycle is disabled.

7.3.3 Contents of the Data Block

The data block to be created must comprise at least 68 words (DW 0 to 67). The number of the selected data block must be entered under parameter DBNR when an FB is called.

DW 0	
DW 1 DW 2 DW 3	**Machine readable product code** of module
DW 4 DW 5 DW 6	**Version of the module firmware**
DW 7	**Version of the module hardware**
DW 8 DW 9 DW 10	**Error messages for hardware and communications errors**
DW 11 DW 12	
DW 13	**Error message for parameter assignment errors**
DW 14 DW 15 DW 16	
DW 17	**Control bits**
DW 18 DW 19	**Status bits**
DW 20 DW 21	**Interrupt request bytes for Channel 1** **Interrupt request bytes for Channel 2**
DW 22	**Hysteresis**
DW 23	**Identifier of configured mode and DB number**
DW 24 DW 25 DW 26 DW 27 DW 28	
DW 29	**Identifiers of the tracks to be transferred**

DW 30 DW 31 DW 32 DW 33	**Actual value (IST) BCD** **Actual value (IST) Binary**
DW 34 DW 35 DW 36 DW 37	**Initial value of Track 1** **Final value of Track 1**
DW 38 DW 39 DW 40 DW 41	**Initial value of Track 2** **Final value of Track 2**
DW 42 DW 43 DW 44 DW 45	**Initial value of Track 3** **Final value of Track 3**
DW 46 DW 47 DW 48 DW 49	**Initial value of Track 4** **Final value of Track 4**
DW 50 DW 51 DW 52 DW 53	**Initial value of Track 5** **Final value of Track 5**
DW 54 DW 55 DW 56 DW 57	**Initial value of Track 6** **Final value of Track 6**
DW 58 DW 59 DW 60 DW 61	**Initial value of Track 7** **Final value of Track 7**
DW 62 DW 63 DW 64 DW 65	**Initial value of Track 8** **Final value of Track 8**
DW 66 DW 67	**Zero offset**

This data is transferred from the DB to the IP 240 and must be adapted beforehand in the DB. The hysteresis is only transferred to the IP 240 during a configuration pass.

If you wish to read the current values of the data areas, you must first call the control FB and initialize it for Read function 1 or 3.

This data is specified by the initializing parameters for the configuring FB or is transferred from the IP 240 to the DB when the module is configured.

These data words are used internally and are not available for any other purpose.

Control bits

Data byte	Bit 7	6	5	4	3	2	1	0
DL 17	AMSK	0	0	0	DA2F	DA2S	DA1F	DA1S
DR 17	0	0	0	0	0	0	0	REFF

AMSK =1 All process interrupts for the channel are masked, i.e. lost
=0 Enable process interrupts

DA2F DA2S
0 0 Digital output D1 is reset
0 1 Digital output D2 is set on the basis of the mode in dependence on the actual value
1 1 Digital output D2 is set irrespective of the actual value

DA1F DA1S
0 0 Digital output D1 is reset
0 1 Digital output D1 is set on the basis of the mode in dependence on the actual value
1 1 Digital output D1 is set irrespective of the actual value

REFF =1 Enable for reference point approach
=0 Normal actual value acquisition

Status bits

Data byte	Bit 7	6	5	4	3	2	1	0
DL 18	DA2	DA1	0	0	0	0	0	0
DR 18	0	0	0	0	SYNC	0	DRBR	NPUE
DL 19	REF8	REF7	REF 6	REF5	REF4	REF3	REF2	REF1
DR 19	0	0	0	0	0	0	UEBL	SG

DA2 =1 Digital output D2 is set
=0 Digital output D2 is not set

DA1 =1 Digital output D1 is set
=0 Digital output D1 is not set

SYNC =1 Reference point approach was terminated with synchronization

DRBR =1 Wirebreak/short-circuit in encoder lines for symmetrical pulse trains

NPUE =1 Number of pulses between two zero mark signals has changed

REFn =1 Actual value (IST) is within Track n (including track limits)
=0 Actual value (IST) is beyond Track n

UEBL =1 Positive or negative range violation of actual value (IST)
(IST < - 99,999 or IST > 99,999)

SG =1 The actual value specified in DW 30/31 and 32/33 is negative
=0 The actual value specified in DW 30/31 and 32/33 is positive

Interrupt request byte for Channel 1 and Channel 2

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 20	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	Channel 1
DR 20	0	0	0	0	0	DRB	NPU	UEB	Channel 1
DL 21	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	Channel 2
DR 21	0	0	0	0	0	DRB	NPU	UEB	Channel 2

RFn =1 Process interrupt was initiated by positive-going edge of corresponding reference bit REFn

DRB =1 Process interrupt was initiated by wire break monitoring

NPU =1 Process interrupt was initiated by zero mark monitor

UEB =1 Process interrupt was initiated by a range violation

Hysteresis

Data byte	Bit 7	6	5	4	3	2	1	0
DL 22	0	0	0	0	0	0	0	0
DR 22	10^1				10^0			

The hysteresis can be specified in the range 0 to 99.
The values entered in DL 22 are not taken into account and do not lead to an error message.

Identifier of the configured mode and data block number

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 23	0	0	0	0	0	0	0	1	
DR 23	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DB no.

After error-free configuring of the channel, a bit combination corresponding to the mode is entered in DL 23.

DL 23 $=01_H$ The channel was configured for position decoding mode
DR 23 = Number of the data block (in binary)

Identifiers of tracks used

Data byte	Bit 7	6	5	4	3	2	1	0
DL 29	0	0	0	0	0	0	0	0
DR 29	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1

TRn =1 The track limits for this track are to be transferred
=0 The track limits for this track are not to be transferred

Actual value (IST) in BCD code

Data byte	Bit 7	6	5	4	3	2	1	0
DL 30	0	0	0	0	0	0	0	0
DR30	0	0	0	0	10^4			
DL 31	10^3				10^2			
DR 31	10^1				10^0			

Actual value (IST) in binary code

Data byte	Bit 7	6	5	4	3	2	1	0
DL 32	0	0	0	0	0	0	0	0
DR 32	0	0	0	0	0	0	0	2^{16}
DL 33	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
DR 33	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The specified values are absolute values. The **sign of the actual values (SG)** is entered in the status area (D 19.0).

Initial value of the first track (ANF 1)

Data byte	Bit 7	6	5	4	3	2	1	0
DL 34	0	0	0	0	0	0	0	SG
DR 34	0	0	0	0	10^4			
DL 35	10^3				10^2			
DR 35	10^1				10^0			

SG =1 The initial value is negative Permissible range: - 99,999 to + 99,999
=0 The initial value is positive

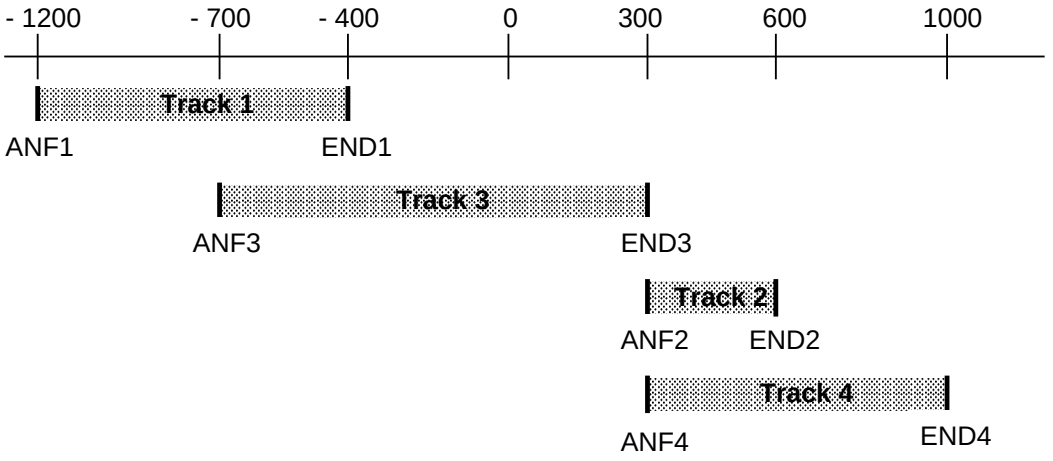
Final value of the first track (END 1)

Data byte	Bit 7	6	5	4	3	2	1	0
DL 36	0	0	0	0	0	0	0	SG
DR 36	0	0	0	0	10^4			
DL 37	10^3				10^2			
DR 37	10^1				10^0			

SG =1 The final value is negative Permissible range: - 99,999 to + 99,999
=0 The final value is positive

DWs 38 to 65 contain the initial and final values of tracks 2 to 8

Example of track limit arrangement:



Note

If an initial track value exceeds the final track value, the corresponding REFn bit is **not** set for any actual value. **No** error message is output when data are transferred.

Zero offset (NVER)

Data byte	Bit 7	6	5	4	3	2	1	0
DL 66	0	0	0	0	0	0	0	SG
DR 66	0	0	0	0	10^4			
DL 67	10^3				10^2			
DR 67	10^1				10^0			

SG =1 The zero offset is negative Permissible range: - 99,999 to + 99,999
=0 The zero offset is positive

7.4 An Example of Position Decoding: Heat Treatment

The induction coil of an induction furnace for heat treatment must move at different speeds over different sections of the workpiece to compensate for cross-section variations and achieve the same hardness over the whole length of the workpiece.

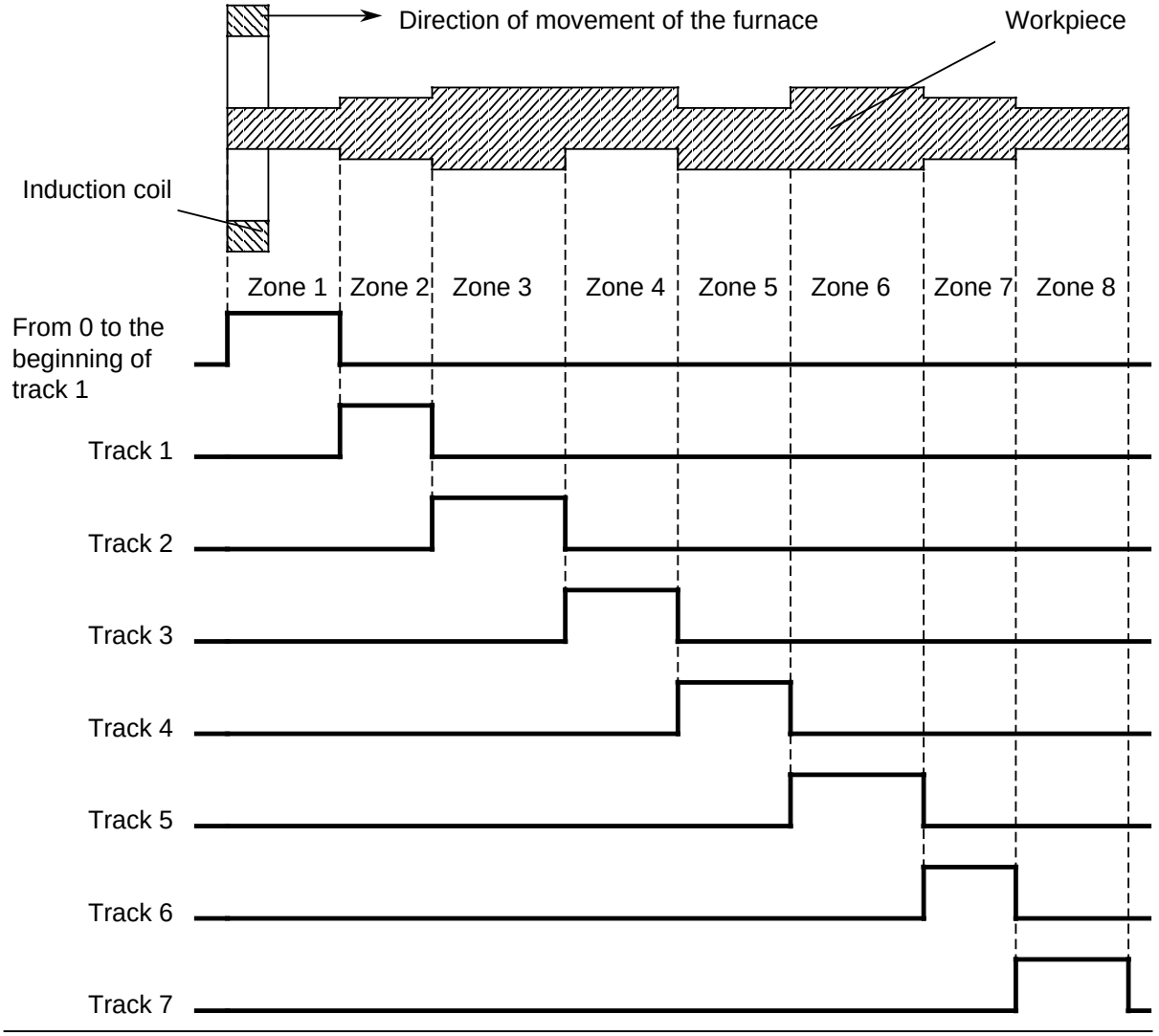


Fig. 7-11. Assignment of the Zones of a Workpiece to Tracks

Track 8 is used to switch off the feed motor at the end of a run and for automatic return to the home position.

Functional description
All data required for operation must be entered in a data block (DB 10 in the example). The data include:
- the speed at which the furnace moves over the various zones of the workpiece,
- the cut-off points of the zones (limit values),
- the identifiers for the various zones,
- the traversing speeds for a new starting point (zero point) and
- the traversing speeds for automatic return of the induction coil to the starting point.

1. Preparatory measures for heat treatment
When the workpiece has been placed in the furnace and the data entered in DB 10, the induction coil must be moved to its starting point. Momentary-contact pushbuttons ”FORWARD” and ”BACK” are used to move the coil to its starting position. The equipment is ready once the ”ON INPUT” pushbutton has been pressed to acknowledge. This state is indicated by the ”ENABLED” indicator.

2. Heat Treatment
Heat treatment is started by pressing the ”START” button. The ”RUNNING” indicator stays on as long as heat treatment is in progress. At the final/turning point, the heater is switched off and the induction coil returns to its starting position. The ”Heating” indicator shows the state of the heater. The process can be repeated when the ”ENABLED” indicator goes on.

3. Aborting heat treatment
The heater is switched off and the induction coil stopped when you press ”EMERGENCY STOP” or limit switch ”LMTSW FORW” or ”LMTSW BACK”. The ”STOPPED” indicator shows which option was used to halt the process, as shown in the following table:

Pushbutton	"EMERGENCY STOP" indicator
EMERGENCY STOP	shows steady light
LMTSW FORW	flashes
LMTSW BACK	flashes

Following an abort, heat treatment cannot be resumed until the induction coil has returned to its home position. To move the coil, proceed as directed in Step 1.

4. Faults
An error on the IP 240 sets the ”FAULT” indicator. Flag byte 10 contains a code indicating the cause of the error.
The following steps are carried out automatically in the event of a fault:
- the heater is switched off
- the induction coil is stopped
- flag byte 11 is transferred to flag byte 10
- flag byte 11 is reset

Stipulations

Input card	→	Module address	4
Output card	→	Module address	12
Analog output card	→	Module address	128 (1st output)
IP 240	→	Module address	144
		(IRA enabled for S5-115U and S5-135U	
		PY 0 enabled for S5-150U)	

Data block 10

- Speeds (in binary)
  KF+ 1024=maximum forward speed
  KF - 1024=maximum backward speed

- Zone limits (BCD code in the range 0 to +99,999)

  e.g. DW 15 KH 0003
  DW 16 KH 5680
  → +35,680 beginning of the third and end of the second zone

The initial and final value of a zone enabled in DR 12 must always be entered: The initial value must be smaller than the final value.

- Bits for the zones used (DR 12)

Bit	Zone	→	Track of the IP 240	
0	1		-	(Zone 1 always exists)
1	2		1	
2	3		2	
3	4		3	
4	5		4	
5	6		5	
6	7		6	
7	8		7	

Inputs, outputs, flags, timers and counters used

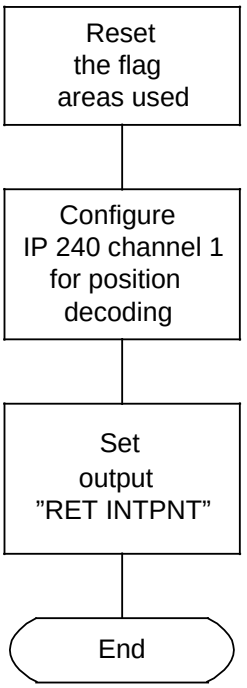
```
OPERAND  SYMBOL       COMMENT

I 4.0    EMERG STOP
I 4.1    START        START RUN
I 4.2    ON INTPNT    TRANSFER OF A NEW INITIAL POSITION
I 4.3    FORWARD      SELECT NEW INITIAL POSITION FOR THE FURNACE
I 4.4    BACK         SELECT NEW INITIAL POSITION FOR THE FURNACE
I 4.6    LMTSW FORW   LIMIT SWITCH FURNACE FORWARD
I 4.7    LMTSW BACK   LIMIT SWITCH FURNACE BACKWARD

Q 12.0   STOPPED      EMERGENCY STOP ACTIVATED
Q 12.1   RUNNING      RUN STARTED
Q 12.2   ENABLED      READY FOR NEXT RUN
Q 12.3   RET INTPNT   BEFORE RESTARTING THE INITIAL POSITION MUST BE TRANSFERRED
Q 12.4   HEATING      HEATING ON (CONTACTOR+INDICATOR)
Q 12.5   FAULT        FAULT MESSAGE FROM CONTROLLER (IP)

F 0.0    ZERO SIGNAL  FLAG ALWAYS HAS SIGNAL STATE ZERO

FY 2     AUX BYTE1    SCRATCH FLAG BYTE CYCLIC PROGRAM
FY 3     AUX BYTE2    SCRATCH FLAG BYTE INTERRUPT SERVICE ROUTINE

FW 4     AUX BYTE1    SCRATCH FLAG WORD - DATA WORD POINTER IN DB10
FW 6     AUX BYTE2    SCRATCH FLAG WORD - DATA WORD POINTER IN DB12
FW 8     AUX BYTE3    SCRATCH FLAG WORD - DATA WORD POINTER IN DB12

FY 10    CHECK BYTE   IMAGE OF FB11 IN CASE OF ERROR

F 11.0   PAFE CONF    FOR CONFIGURATION                          (FB20)
F 11.1   PAFE ACT1    FOR READING ACTUAL VALUE AND STATUS BITS   (FB23)
F 11.2   PAFE ACT2    FOR READING ACTUAL VALUE AND STATUS BITS   (FB25)
F 11.3   PAFE IR      FOR READING INTERRUPT REQUEST BYTE         (FB27)
F 11.4   PAFE TRAC1   FOR WRITING TRACK LIMITS                   (FB24)
F 11.5   PAFE ZERO    FOR WRITING ZERO OFFSET                    (FB23)
F 11.6   PAFE TRAC8   FOR WRITING TRACK LIMITS                   (FB25)
F 11.7   WIRE BREAK   WIREBREAK/SHORT-CIRCUIT IN ENCODER         (FB28)

F 12.1   EDGE         EDGE FLAG OF I "ON INTPNT"
F 12.2   FORW ACTIV   FORWARD TRAVERSING PROGRAM ACTIVE
F 12.4   BACK-AKTIV   BACKWARD TRAVERSING PROGRAM ACTIVE

F 12.6   FIN POINT    FINAL POSITION OF FORWARD TRAVERSING PROGRAM REACHED
F 12.7   INT POINT    INITIAL POINT/STARTING POSITION

FW 14    ANALOG VAL   ANALOG VALUE TO BE OUTPUT IN UNITS (MAX 1024)
FW 16    AUX WORD4    AUXILIARY FLAG WORD - INTERRUPT SERVICE ROUTINE (STATUS BITS)

T 1      is used to generate a flashing frequency
C 1      is used to generate a flashing frequency
```

```
DB10                                                LEN=38

 0:     KH = 0000;
 1:     KF = +00250;                    Forward speed on initial point selection
 2:     KF = -00250;                    Backward speed on initial point selection
 3:     KF = +00750;                    Traversing speed in zone 1
 4:     KF = +00320;                    Traversing speed in zone 2
 5:     KF = +00600;                    Traversing speed in zone 3
 6:     KF = +01024;                    Traversing speed in zone 4
 7:     KF = +00100;                    Traversing speed in zone 5
 8:     KF = +00500;                    Traversing speed in zone 6
 9:     KF = +00700;                    Traversing speed in zone 7
10:     KF = +00800;                    Traversing speed in zone 8
11:     KF = -00500;                    Backward speed to initial point
12:     KM = 0000000011111111;          Bits of the zones used: right byte
13:     KH = 0001;                      ] Beginning zone 2 = End zone 1
14:     KH = 0400;                      ]        (Beginning zone 1 = 0)
15:     KH = 0002;                      } Beginning zone 3 = End zone 2
16:     KH = 2000;                      }
17:     KH = 0002;                      ] Beginning zone 4 = End zone 3
18:     KH = 6000;                      ]
19:     KH = 0003;                      } Beginning zone 5 = End zone 4
20:     KH = 4000;                      }
21:     KH = 0003;                      ] Beginning zone 6 = End zone 5
22:     KH = 5000;                      ]
23:     KH = 0004;                      } Beginning zone 7 = End zone 6
24:     KH = 6000;                      }
25:     KH = 0006;                      ] Beginning zone 8 = End zone 7
26:     KH = 7000;                      ]
27:     KH = 0007;                      } Switchoff point for heating and
28:     KH = 4000;                      } turning point to return to home
29:     KS ='End';                        position
31:     KH = 0000;                        (end zone 8 or last valid zone)
32:     KH = 0000;
33:
```

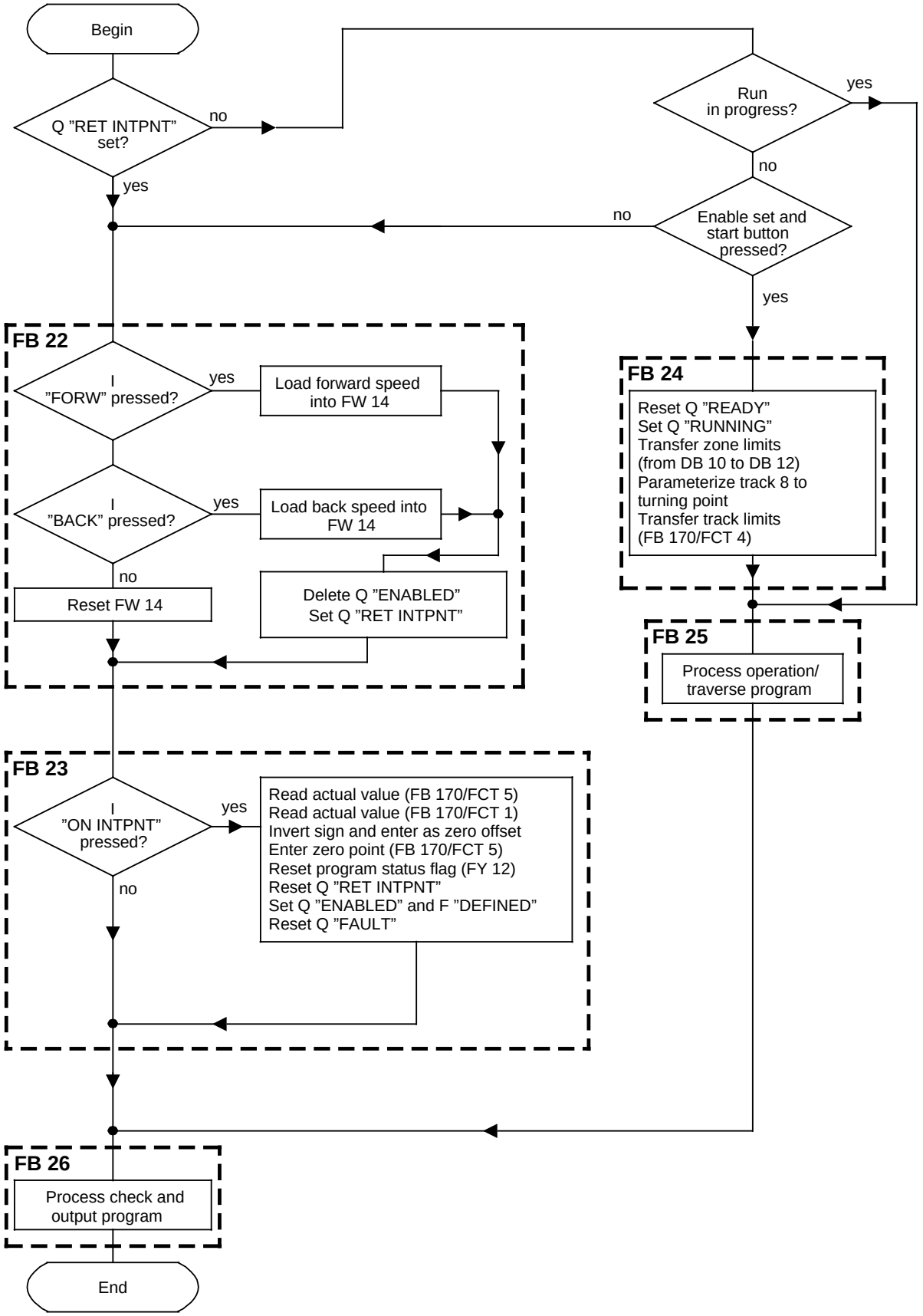
```
DB12                                                LEN=73

 0:     KH = 0000;
 1:     KS ='      ';                  MACHINE-READABLE PRODUCT CODE OF THE MODULE
 4:     S  ='      ';                  Version of the firmware
 7:     KS ='  ';                      Hardware version
 8:     KH = 0000;                     Error flags for
 9:     KH = 0000;                     hardware and
10:     KH = 0000;                     communications errors
11:     KH = 9001;
12:     KH = 00FF;
13:     KH = 0000;                     Parameter assignment error message
14:     KH = 0000;
15:     KH = FF05;
16:     KH = 0080;
17:     KM = 0000000000000000;         Control bits
18:     KM = 0000000000000000;         Status bits
19:     KM = 1000000000000001;         Status bits (RF1-REF8)
20:     KM = 1000000000000000;         Interrupt request byte channel 1
21:     KM = 0000000000000000;         Interrupt request byte channel 2
22:     KH = 0000;                     Hysteresis
23:     KY = 001,012;                  Mode and DB number
24:     KH = 0000;
25:     KH = 0000;
26:     KH = 0000;
27:     KH = 0000;
28:     KH = 0000;
29:     KM = 0000000010000000;         Bits for tracks to used
30:     KH = 0000;                     Actual value in BCD code
31:     KH = 1942;
32:     KM = 0000000000000000;         Actual value in binary code
33:     KM = 0000011110010110;
34:     KH = 0001;                     Initial value track 1
35:     KH = 0400;
36:     KH = 0002;                     Final value
37:     KH = 2000;
38:     KH = 0002;                     Initial value track 2
39:     KH = 2000;
40:     KH = 0002;                     Final value
41:     KH = 6000;
42:     KH = 0002;                     Initial value track 3
43:     KH = 6000;
44:     KH = 0003;                     Final value
45:     KH = 4000;
46:     KH = 0003;                     Initial value track 4
47:     KH = 4000;
48:     KH = 0003;                     Final value
49:     KH = 5000;
50:     KH = 0003;                     Initial value track 5
51:     KH = 5000;
52:     KH = 0004;                     Final value
53:     KH = 6000;
54:     KH = 0004;                     Initial value track 6
55:     KH = 6000;
56:     KH = 0006;                     Final value
57:     KH = 7000;
58:     KH = 0006;                     Initial value track 7
59:     KH = 7000;
60:     KH = 0007;                     Final value
61:     KH = 4000;
62:     KH = 0109;                     Initial value track 8
63:     KH = 9999;
64:     KH = 0000;                     Final value
65:     KH = 0000;
66:     KH = 0100;                     Zero offset value
67:     KH = 7450;
68:
```

```
DB20                                                LEN=35

 0:     KH = 0000;
 1:     KH = 0000;
 2:     KH = 0000;
 3:     KH = 0000;
 4:     KH = 0000;
 5:     KH = 0000;
 6:     KH = 0000;
 7:     KH = 0000;
 8:     KH = 0000;
 9:     KH = 0000;
10:     KH = 0000;
11:     KH = 0000;
12:     KH = 0000;
13:     KH = 0000;
14:     KH = 0000;
15:     KH = 0000;
16:     KH = 0000;
17:     KH = 0000;
18:     KH = 0000;
19:     KH = 0000;
20:     KH = 0000;
21:     KH = 0000;
22:     KH = 0000;
23:     KH = 0000;
24:     KH = 0000;
25:     KH = 0000;
26:     KH = 0000;
27:     KH = 0000;
28:     KF = +00000;                    DATA WORD POINTER
29:     KF = +00000;                    FLAG WORD POINTER
30:

DB38                                                LEN=35

 0:     KH = 0000;
 1:     KH = 0000;
 2:     KH = 0000;
 3:     KH = 0000;
 4:     KH = 0000;
 5:     KH = 0000;
 6:     KH = 0000;
 7:     KH = 0000;
 8:     KH = 0000;
 9:     KH = 0000;
10:     KH = 0000;
11:     KH = 0000;
12:     KH = 0000;
13:     KH = 0000;
14:     KH = 0000;
15:     KH = 0000;
16:     KH = 0000;
17:     KH = 0000;
18:     KH = 0000;
19:     KH = 0000;
20:     KH = 0000;
21:     KH = 0000;
22:     KH = 0000;
23:     KH = 0000;
24:     KH = 0000;
25:     KH = 0000;
26:     KH = 0000;
27:     KH = 0000;
28:     KF = +00000;                    DATA WORD POINTER
29:     KF = +00000;                    FLAG WORD POINTER
30:
```

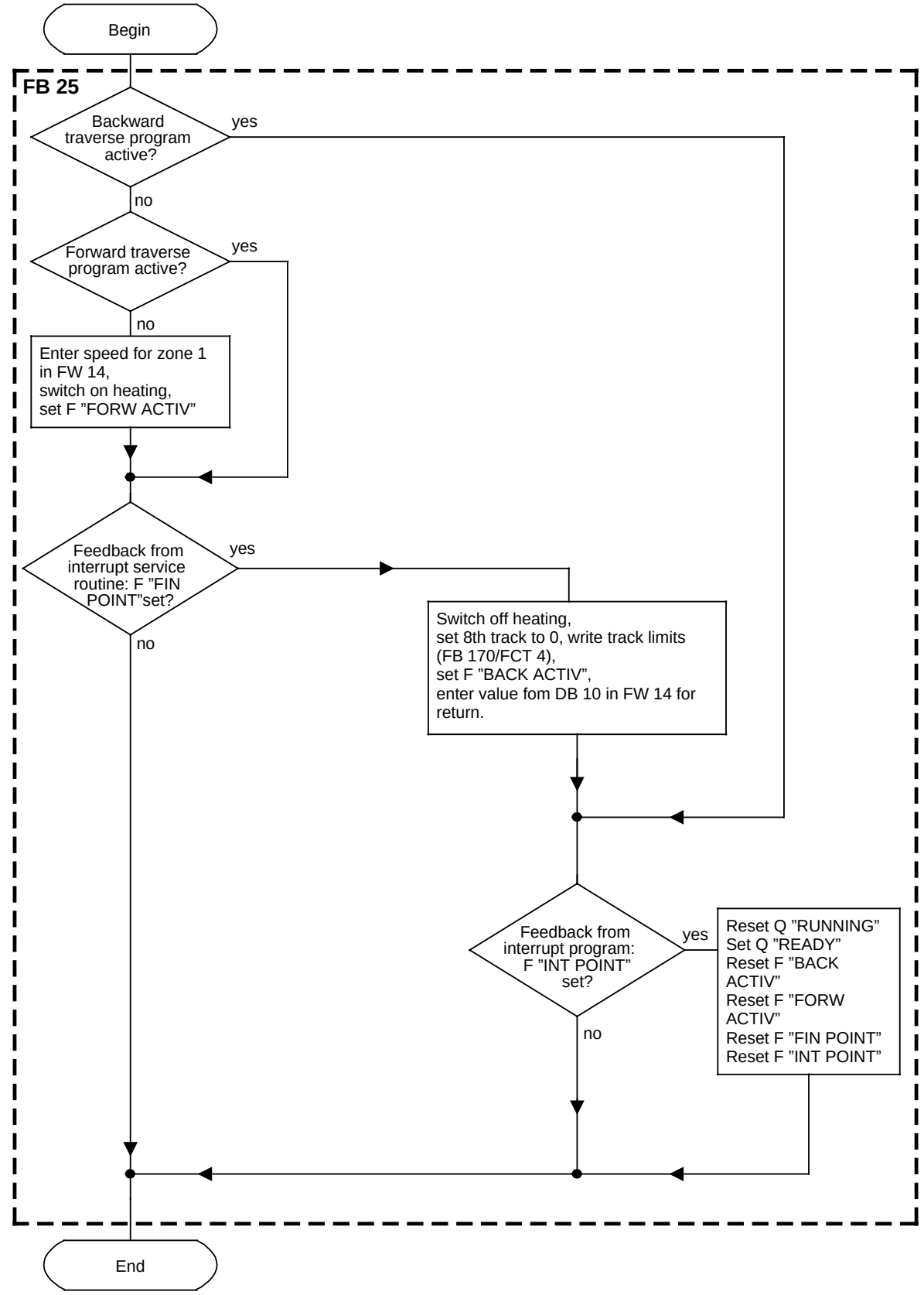
Start routine FB 20



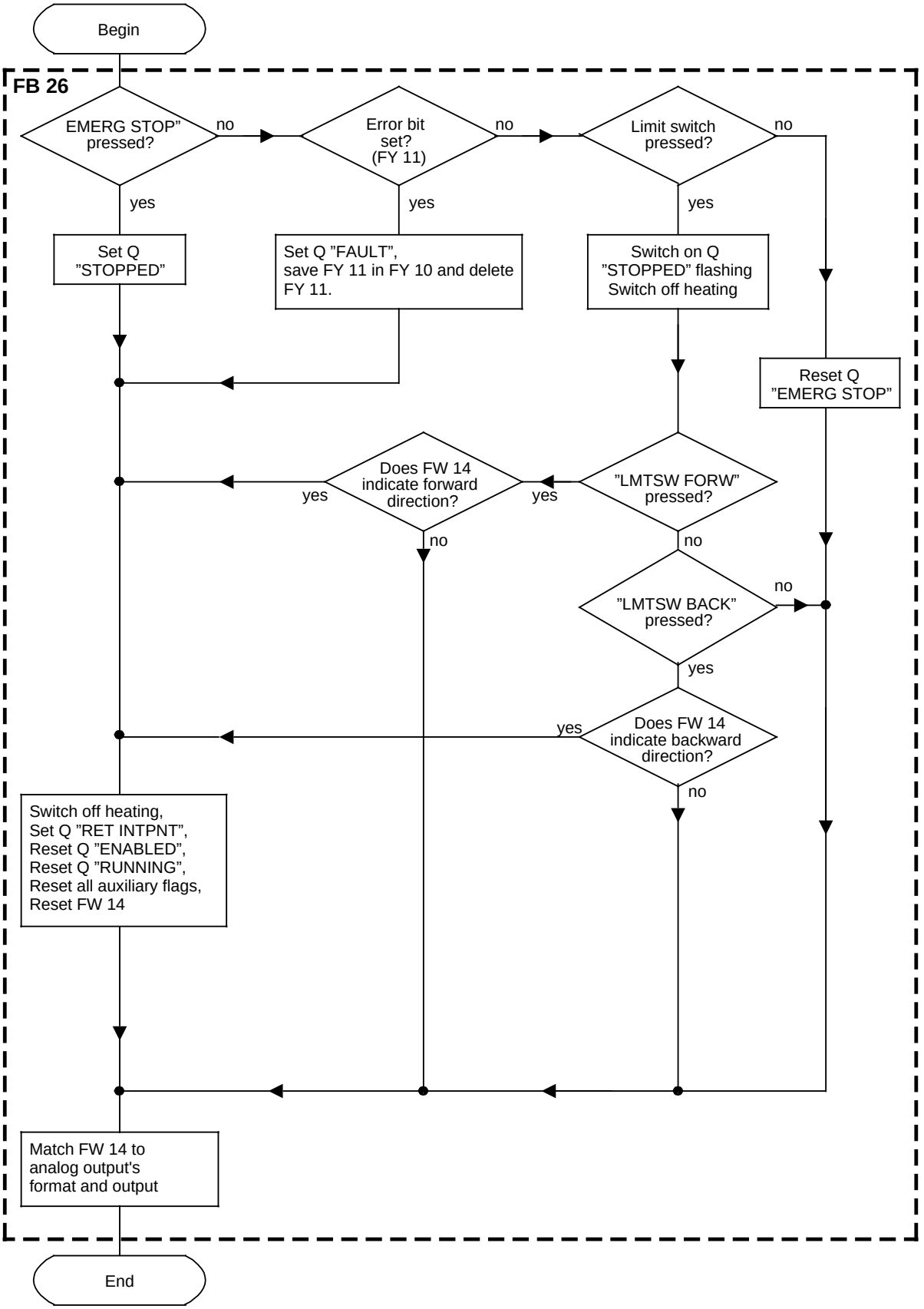
Cyclic program FB 21



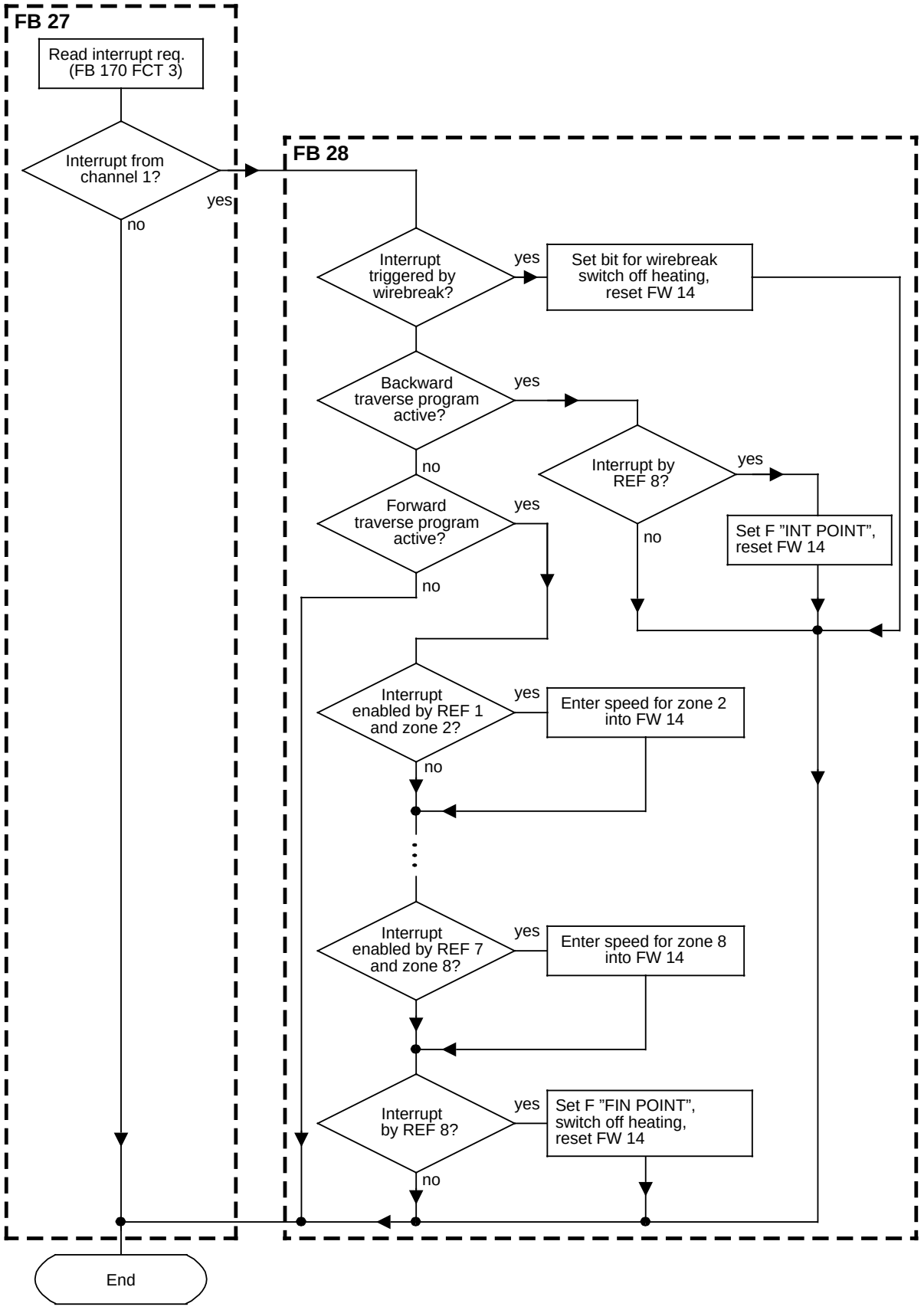
Operation/traverse program FB 25



Control and output program FB 26



Interrupt service routine FB 27 and FB 28



```
OB 1                                                        LEN=8

NETWORK  1     0000          CYCLE
0000      :JU  FB  21
0001 NAME :IP PROG
0002      :BE


OB 2                                                        LEN=16

NETWORK  1     0000          PROCESS INTERRUPT PROGRAM
0000      :JU  FB  38                      SAVE SCRATCH FLAGS
0001 NAME :FLAG.SAV
0002 DBNR :    DB  38
0003      :
0004      :JU  FB  27                      INTERRUPT SERVICE ROUTINE FOR THE IP 240
0005 NAME :INTERPT
0006      :
0007      :JU FB  39                       WRITE SCRATCH FLAGS
0008 NAME :LOAD.FLG
0009 DBNR :    DB  38
000A      :BE
```

FB 38 and FB 39 are not required in the S5-150U, S5-155U (150U mode) or S5-135U (when set for interrupts at block boundaries).

```
OB 20     (in S5-115U: OB 21)                               LEN=9

NETWORK  1     0000          MANUAL RESTART
0000      :
0001      :JU  FB  20                     CONFIGURE THE IP 240 CHANNEL 1
0002 NAME :CONFIG
0003      :BE


OB 22                                                       LEN=17

NETWORK  1     0000          RESTART AFTER POWER OFF
0000      :
0001      :JU  FB  38                      SAVE SCRATCH FLAGS (FY200-255)
0002 NAME :FLAG.SAV
0003 DBNR :    DB  20
0004      :
0005      :JU  FB  20                      CONFIGURE THE IP 240 CHANNEL
0006 NAME :CONFIG
0007      :
0008      :JU  FB  39                      RELOAD SCRATCH FLAGS
0009 NAME :LOAD.  FLG
000A DBNR :    DB  20
000B      :BE
```

FB 38 and FB 39 are not required in the S5-115U, S5-155U, or the S5-135U when set for ”automatic restart on power-up” in DX0.

```
FB 20                                                    LEN=52

NETWORK 1      0000          CONFIGURE IP 240 CHANNEL 1

FB20 : CONFIGURE CHANNEL 1 AND PRESET PROGRAM FLAGS

CHANNEL 1 OF THE IP240 IS CONFIGURED FOR POSITION DECODING MODE AND PROVIDED
WITH INTERRUPT IDS.
THE FLAG AREAS USED BY THE PROGRAM ARE FIRST RESET AND THEN PRESET.

NAME :CONFIG

0005      :L   KH 0000                        RESET FLAG AREAS USED IN
0007      :T   FW   0                         SAMPLE PROGRAM
0008      :T   FW   2                         AUXILIARY FLAG BYTES
0009      :T   FW   4    -AUX WORD1           DB-POINTER
000A      :T   FW   6    -AUX WORD2           DB-POINTER
000B      :T   FW   8    -AUX WORD3           DB-POINTER
000C      :T   FW  16    -AUX WORD4           (INTERRUPT REQUEST BYTE CHANNEL 1)
000D      :T   FW  10                         AUXILIARY FLAG (PAFE BITS)
000E      :T   FW  12                         AUXILIARY FLAG (PROGRAM STATUS)
000F      :T   FW  14    -ANALOG VAL          ANALOG VALUE FOR OUTPUT
0010      :C   DB  12
0011      :L   KH 00FF                        STORE THE BITS FOR THE RESERVED
0013      :T   DR  29                         TRACKS (TRACK1-8) IN THE DB
0014      :JU FB 169
0015 NAME :STRU.WEG
0016 BGAD :    KF +144                        MODULE ADDRESS 144
0017 KANR :    KF +1                          CHANNEL NUMBER 1
0018 DBNR :    KF +12                         DATA BLOCK NUMBER 1
0019 AFL  :    KF +1                          RESOLUTION OF THE ENCODER PULSES
001A IMP  :    KF +10                         ENCODER PULSE NUMBER DIVISIBLE BY 5
001B DIG1 :    KM 00000000 00000000           DIG 1 NOT USED
001C DIG2 :    KM 00000000 00000000           DIG 2 NOT USED
001D PRA1 :    KM 00000000 11111111           PROCESS INTERRUPTS FOR REF1 - REF8
001E PRA2 :    KM 00000000 00000100           PROCESS INTERRUPT ON WIRE-BREAK
001F PAFE :    FY   2    -AUX BYTE1           PARAMTER ASSIGNMENT ERROR BYTE
0020 BER  :    KF +0                          "0"= I/O AREA (NOT USED FOR 115U)
0021 ABIT :    KY 0,0                         RESET SYSTEM DATA RS 0.0
0022      :                                   ON CALLING FB 170/FCT 3
0023      :                                   (150U ONLY)
0024      :
0025      :L   FY   2    -AUX BYTE1           SCAN FOR ERROR
0026      :L   KH 0000
0028      :><F
0029      :S   F   11.0  -PAFE CONF           CONFIGURING ERROR
002A      :
002B      :AN  Q   12.3  -RET INTPNT
002C      :S   Q   12.3  -RET INTPNT          REQUEST FOR INITIAL POINT
002D      :                                   SETTING
002E      :BE

FW   4   = AUX WORD1              SCRATCH FLAG WORD - DATA WORD POINTER IN DB10
FW   6   = AUX WORD2              SCRATCH FLAG WORD - DATA WORD POINTER IN DB12
FW   8   = AUX WORD3              SCRATCH FLAG WORD - DATA WORD POINTER IN DB12
FW  16   = AUX WORD4              AUXIL. FLAG WORD - INTERRUPT SERVICE ROUT.(STATUS BITS)
FW  14   = ANALOG VAL             ANALOG VALUE TO BE OUTPUT IN UNITS (MAX 1024)
FY   2   = AUX BYTE1              SCRATCH FLAG BYTE CYCLIC PROGRAM
F   11.0 = PAFE CONF              FOR CONFIGURING              (FB20)
Q   12.3 = RET INTPNT             INITIAL POINT MUST BE TRANSFERRED BEFORE RESTARTING
```

```
FB 21                                                        LEN=33

NETWORK 1     0000          ORGANIZATION PROGRAM

FB21 : ORGANIZATION PROGRAM

FB21 IS THE ORGANIZATION BLOCK FOR THE SAMPLE PROGRAM

NAME :IP PROG

0005      :A   Q   12.3  -RET INTPNT
0006      :JC =FOR1                          INITIAL POINT SELECTION PROGRAM
0007      :A   Q   12.1  -RUNNING
0008      :JC =FOR3                          TRAVERSING PROGRAM
0009      :A   Q   12.2  -ENABLE
000A      :A   I    4.1  -START
000B      :JC =FOR2                          START PROGRAM
000C FOR1 :
000D      :JU FB  22                         REDEFINE INITIAL POINT
000E NAME :SELECT
000F      :JU FB  23                         TRANSFER INITIAL POINT
0010 NAME :OFFSET
0011      :JU =CHECK                         CHECK/SWITCHOFF PROGRAM
0012 FOR2 :
0013      :JU FB  24                         ACTIVATE RUN PROGRAM
0014 NAME :START
0015 FOR3 :
0016      :JU FB  25                         TRAVERSING PROGRAM OF THE FURNACE
0017 NAME :OPERATE
0018 CHEK :
0019      :JU FB  26                         EVALUATION OF STOP REQUESTS
001A NAME :CHECK
001B      :BE

Q   12.3 = RET INTPNT            THE INITIAL POINT MUST BE TRANSFERRED BEFORE RESTARTING
Q   12.1 = RUNNING               RUN STARTED
Q   12.2 = ENABLED               A NEW RUN POSSIBLE
I    4.1 = START                 START RUN
```

```
FB 22                                                          LEN=34

NETWORK 1     0000          REDEFINE INITIAL POINT

FB22 : REDEFINE/ADJUST INITIAL POINT OF THE FURNACE

AS LONG AS ONE OF THE TWO KEYS IS PRESSED, THE FURNACE IS MOVED IN ONE OF THE TWO
DIRECTIONS WITH THE SPEED STORED IN DB10 (DW1/DW2).

AFTER THE FURNACE HAS TRAVERSED, THE NEW INITIAL POSITION MUST BE TRANSFERRED
(I "ON INTPNT") OR THE FURNACE MUST RETURN TO ITS OLD INITIAL POINT (I "TO INTPNT")
BEFORE ANOTHER AUTOMATIC RUN IS POSSIBLE.

NAME :SELECT

0005      :AN  I    4.3  -FORWARD             IF NONE OR BOTH BUTTONS ARE
0006      :AN  I    4.4  -BACK                PRESSED THEN RESET ANALOG
0007      :O(                                 VALUE, END
0008      :A   I    4.3  -FORWARD    01
0009      :A   I    4.4  -BACK       01
000A      :)                          01
000B      :JC =ZERO
000C      :C   DB  10
000D      :A   I    4.3  -FORWARD
000E      :JC =DW1
000F      :A   I    4.4  -BACK
0010      :JC =DW2
0011 ZERO :L   KB 0                           RESET SPEED
0012      :T   FW  14    -ANALOG VAL
0013      :BEU
0014 DW1  :L   DW   1                         TRANSFER SPEED
0015      :T   FW  14    -ANALOG VAL
0016      :JU =SIGN
0017 DW2  :L   DW   2                         TRANSFER BACKWARD SPEED
0018      :T   FW  14    -ANALOG VAL
0019 SIGN :AN  F    0.0  -ZERO SIGNAL
001A      :R   Q   12.2  -ENABLED
001B      :S   Q   12.3  -RET INTPNT
001C      :BE

I    4.3 = FORWARD                SELECT NEW INITIAL POINT FOR FURNACE
I    4.4 = BACK                   SELECT NEW INITIAL POINT FOR FURNACE
FW  14   = ANALOG VAL             ANALOG VALUE TO BE OUTPUT IN UNITS (MAX 1024)
F    0.0 = ZERO SIGNAL            FLAG ALWAYS RETAINS SIGNAL STATE ZERO
Q   12.2 = ENABLED                NEW RUN POSSIBLE
Q   12.3 = RET INTPNT             THE INITIAL POINT MUST BE TRANSFERRED BEFORE RESTARTING
```

```
FB 23                                                    LEN=75

NETWORK 1     0000          TRANSFER OF INITIAL POINT

FB23 : TRANSFER INITIAL POINT

WHEN INPUT ”ON INTPNT” IS ACTIVATED, THE ACTUAL VALUE IS READ
AND SET TO ZERO BY A ZERO OFFSET

NAME :OFFSET

0005      :ON  I    4.2  -ON INTPNT
0006      :O   F   12.1  -EDGE                EDGE FLAG
0007      :JC =END
0008      :C   DB  12
0009      :L   KB 0                           REVOKE OLD
000A      :T   DW  66                         ZERO OFFSET
000B      :T   DW  67
000C      :JU FB 170
000D NAME :STEU.WEG
000E DBNR :    KF +12
000F FKT  :    KF +5                          WRITE ZERO OFFSET
0010 PAFE :    FB   2    -AUX BYTE1
0011      :L   KH 0000
0013      :L   FB   2    -AUX BYTE1
0014      :><F
0015      :=   F   11.5  -PAFE ZERO
0016      :JU FB 170
0017 NAME :STEU.WEG
0018 DBNR :    KF +12
0019 FKT  :    KF +1                          READ ACTUAL VALUE AND STATUS BITS
001A PAFE :    FY   2    -AUX BYTE1
001B      :L   KH 0000
001D      :L   FY   2    -AUX BYTE1
001E      :><F
001F      :=   F   11.1  -PAFE ACT1           READ ERROR IN ACTUAL VALUE
0020      :
0021      :C   DB  12
0022      :L   DR  19                         STATUS BITS (SIGN)
0023      :L   KH 0001
0025      :AW
0026      :T   FY   2    -AUX BYTE1
0027      :AN  F    2.0                       INVERT SIGN
0028      :=   F    2.0
0029      :L   FY   2    -AUX BYTE1
002A      :T   DL  66                         SG ZERO OFFSET
002B      :L   DR  30                         ACTUAL VALUE 4TH DECADE
002C      :T   DR  66                         4TH DECADE ZERO OFFSET
002D      :L   DW  31                         ACTUAL VALUE 3D, 2ND, 1ST AND 0 DECADES
002E      :T   DW  67                         ZERO OFFSET
002F      :
0030      :JU FB 170
0031 NAME :STEU.WEG
0032 DBNR :    KF +12
0033 FKT  :    KF +5                          WRITE ZERO OFFSET
0034 PAFE :    FB   2    -AUX BYTE1
0035      :L   KH 0000
0037      :L   FY   2    -AUX BYTE1
0038      :><F
0039      :=   F   11.5  -PAFE ZERO           WRITE ERROR ON ZERO OFFSET
003A      :
003B      :L   KH 0000                        RESET PROGRAM FLAGS
003D      :T   FY  12
003E      :AN  F    0.0  -ZERO SIGNAL
003F      :R   Q   12.3  -RET INTPNT
0040      :S   Q   12.2  -ENABLED
```

```
FB 23                                                    LEN=75

0041      :R   Q   12.5  -FAULT
0042 END
0043      :A   I    4.2  -ON INTPNT
0044      :=   F   12.1  -EDGE                SET EDGE FLAG
0045      :BE

I    4.2 = ON INTPNT               TRANSFER OF THE NEW INITIAL POINT
F   12.1 = EDGE                    EDGE FLAG OF I "ON INTPNT"
FY   2   = AUX BYTE1               SCRATCH FLAG CYCLIC PROGRAM
F   11.5 = PAFE ZERO               FOR WRITING ZERO OFFSET                    (FB23)
F   11.1 = PAFE ACT1               FOR READING ACTUAL VALUE AND STATUS BITS   (FB23)
F    0.0 = ZERO SIGNAL             FLAG ALWAYS RETAINS SIGNAL STATE ZERO
Q   12.3 = RET INTPNT              INITIAL POINT MUST BE TRANSFERRED BEFORE RESTARTING
Q   12.2 = ENABLED                 NEW RUN POSSIBLE
Q   12.5 = FAULT                   ERROR MESSAGE FROM THE CONTROLLER (IP)
```

```
FB 24                                                          LEN=97

NETWORK 1     0000          START RUN

FB24 : START RUN / TRANSFER TRACK LIMIT VALUES

FB 24 TRANSFERS THE TRACK LIMIT VALUES STORED IN DB10 (DW12 - DW28)
TO THE WORKING DATA BLOCK OF THE IP 240 AND THEN, USING FB170, TO THE
IP 240.

NAME :START

0005      :AN  F    0.0  -ZERO SIGNAL
0006      :R   Q   12.2  -ENABLED
0007      :S   Q   12.1  -RUNNING
0008      :
0009      :L   KF +15                          PRESET FLAG WORDS
000B      :T   FW   4    -AUX WORD1
000C      :L   KF +36
000E      :T   FW   6    -AUX WORD2
000F      :I        2
0010      :T   FW   8    -AUX WORD3
0011      :L   KB 0
0012      :T   FY   2    -AUX BYTE1
0013      :
0014      :C   DB  10
0015      :L   DR  12                          BITS FOR ZONES
0016      :SRW      1                          ADAPTATION TO BITS FOR THE TRACKS
0017      :L   KH 0080                         SET BITS FOR TRACK 8 TO 1
0019      :OW
001A      :C   DB  12
001B      :T   DR  29
001C      :
001D      :C   DB  10
001E      :L   DW  13                          INITIAL VALUE ZONE 2 (4TH DECADE)
001F      :C   DB  12
0020      :T   DW  34                          -> INT. TRACK 1
0021      :C   DB  10
0022      :L   DW  14                          INT.ZONE 2 (3RD 2ND AND 1ST DECADE)
0023      :C   DB  12
0024      :T   DW  35                          -> INT. TRACK 1
0025      :
0026 BACK :C   DB  10
0027      :DO  FW   4    -AUX WORD1
0028      :L   DW   0                          INT. VALUE TRACK X
0029      :C   DB  12
002A      :DO  FW   6    -AUX WORD2
002B      :T   DW   0                          -> FINAL VALUE TRACK X-1
002C      :DO  FW   8    -AUX WORD3
002D      :T   DW   0                          -> INT. VALUE TRACK X
002E      :
002F      :L   FW   4    -AUX WORD1           INCREMENT COUNTER
0030      :I        1
0031      :T   FW   4    -AUX WORD1
0032      :L   FW   6    -AUX WORD2
0033      :I        1
0034      :T   FW   6    -AUX WORD2
0035      :I        2
0036      :T   FW   8    -AUX WORD3
0037      :
0038      :AN  F    2.0
0039      :=   F    2.0
003A      :A   F    2.0                        RUN TWICE ?
003B      :JC =BACK                            IF NOT, RETURN
003C      :
003D      :L   FW   4    -AUX WORD1
```

```
FB 24                                                          LEN=97

003E      :L   KF +28                        TRANSFER DW13 - 28 ?
0040      :>F
0041      :JC =FOR1
0042      :
0043      :L   FW   6    -AUX WORD2          INCREMENT COUNTER BY 2
0044      :I        2
0045      :T   FW   6    -AUX WORD2
0046      :I        2
0047      :T   FW   8    -AUX WORD3
0048      :JU =BACK
0049 FOR1 :
004A      :C   DB  12
004B      :L   KH 0009
004D      :T   DW  64                        FINAL VALUE TRACK 8 (4TH DECADE)
004E      :L   KH 9999                       (MAX. VALUE)
0050      :T   DW  65                        FINAL VALUE TRACK 8 (3RD, 2ND AND 1ST DECADE)
0051      :
0052      :JU FB 170
0053 NAME :STEU.WEG
0054 DBNR :    KF +12
0055 FKT  :    KF +4                          WRITE TRACK LIMITS
0056 PAFE :    FY   2    -AUX BYTE1
0057      :L   FY   2    -AUX BYTE1
0058      :L   KB 0
0059      :><F
005A      :=   F   11.4  -PAFE-TRAC1         PAFE FOR WRITING TRACK LIMITS
005B      :BE

F    0.0 = ZERO SIGNAL            FLAG ALWAYS RETAINS SIGNAL STATE 0
Q   12.2 = ENABLED                NEW RUN POSSIBLE
Q   12.1 = RUNNING                RUN STARTED
FW   4   = AUX WORD1              SCRATCH FLAG WORD - DATA WORD POINTER IN DB10
FW   6   = AUX WORD2              SCRATCH FLAG WORD - DATA WORD POINTER IN DB12
FW   8   = AUX WORD3              SCRATCH FLAG WORD - DATA WORD POINTER IN DB12
FY   2   = AUX BYTE1              SCRATCH FLAG BYTE CYCLIC PROGRAM
F   11.4 = PAFE TRAC1             FOR WRITING TRACK LIMITS      (FB24)
```

```
FB 25                                                        LEN=67

NETWORK 1     0000          OPERATION / TRAVERSE PROGRAM

FB25 : OPERATION / TRAVERSE PROGRAM OF THE INDUCTION FURNACE

FB25 ENTERS THE INITIAL OR RETURN SPEED OF THE FURNACE
INTO FW14 AND PARAMETERIZES A CONTROL TRACK (TRACK 8), IF
NECESSARY, TO MOVE THE FURNACE BACK TO ITS ORIGINAL POSITION.

NAME :OPERATE

0005      :A   F   12.4  -BACK ACTIV
0006      :JC  =R-PR
0007      :A   F   12.2  -FORW ACTIV
0008      :JC  =FOR1
0009      :C   DB  10
000A      :L   DW   3                          OUTPUT SPEED ZONE 1
000B      :T   FW  14    -ANALOG VAL
000C      :AN  F   12.2  -FORW ACTIV
000D      :S   F   12.2  -FORW ACTIV
000E      :S   Q   12.4  -HEATING             SWITCH ON HEATING
000F      :
0010 FOR1 :A   F   12.6  -FIN POINT           FEEDBACK FROM INTERRUPT SERVICE ROUTINE
0011      :R   Q   12.4  -HEATING             SWITCH OFF HEATING
0012      :JC  =FOR2
0013      :BEU
0014 FOR2 :
0015      :C   DB  12
0016      :L   KB 0
0017      :T   DW  64                          SET FINAL VALUE TRACK 8
0018      :T   DW  65                          TO ZERO
0019      :L   KH 0109
001B      :T   DW  62                          SET INITIAL VALUE
001C      :L   KH 9999                         TO -99999
001E      :T   DW  63
001F      :L   KH 0080                         BITS FOR TRACKS USED
0021      :T   DR  29                          (ONLY TRACK 8 RELEVANT)
0022      :JU  FB 170
0023 NAME :STEU.WEG
0024 DBNR :    KF +12
0025 FKT  :    KF +4                          WRITE TRACK LIMITS
0026 PAFE :    FY   2    -AUX BYTE1
0027      :L   FY   2    -AUX BYTE1
0028      :L   KB 0
0029      :><F
002A      :=   F   11.6  -PAFE TRAC8           PAFE FOR WRITING TRACK LIMITS
002B      :
002C      :C   DB  10
002D      :L   DW  11
002E      :T   FW  14    -ANALOG VAL
002F      :AN  F   12.4  -BACK ACTIV
0030      :S   F   12.4  -BACK ACTIV           SET SCRATCH FLAGS
0031 R-PR :
0032      :A   F   12.7  -INT POINT            FEEDBACK FROM INTERRUPT SERVICE ROUTINE
0033      :JC  =KSET
0034      :BEU
0035 KSET :
0036      :AN  F    0.0  -ZERO SIGNAL
0037      :R   Q   12.1  -RUNNING
0038      :S   Q   12.2  -ENABLED
0039      :R   F   12.2  -FORW ACTIV
003A      :R   F   12.4  -BACK ACTIV
003B      :R   F   12.6  -FIN POINT
003C      :R   F   12.7  -INT POINT
003D
```

```
FB 25                                                    LEN=67

F   12.4 = BACK ACTIV              BACKWARD TRAVERSE PROGRAM ACTIVE
F   12.2 = FORW ACTIV              FORWARD TRAVERSE PROGRAM ACTIVE
FW  14   = ANALOG VAL              ANALOG VALUE TO BE OUTPUT IN UNITS (MAX. 1024)
Q   12.4 = HEATING                 HEATING ON (CONTACTOR + INDICATOR)
F   12.6 = FIN POINT               FINAL POINT OF THE FORWARD TRAVERSE PROGRAM REACHED
F   12.3 = BACK START              BACKWARD TRAVERSE PROGRAM STARTED
FY   2   = AUX BYTE1               SCRATCH FLAG BYTE CYCLIC PROGRAM
F   11.6 = PAFE TRAC8              FOR WRITING TRACK LIMITS          (FB25)
F   12.7 = INT POINT               INITIAL POINT/ORIGINAL POSITION REACHED
F    0.0 = ZERO SIGNAL             FLAG ALWAYS RETAINS SIGNAL STATE ZERO
Q   12.1 = RUNNING                 RUN STARTED
Q   12.2 = ENABLED                 NEW RUN POSSIBLE
```

```
FB 26                                                    LEN=75

NETWORK 1     0000          ERROR/INTERRUPTION CONTROL

FB26 : CONTROL PROGRAM FOR EMERGENCY STOP, MALFUNCTIONS OR LIMIT SWITCHES

FB26 QUERIES INPUTS ”EMERG STOP”, ”LMTSW FORW” AND ”LMTSW BACK”
AND RESPONDS TO PARAMETER ASSIGNMENT ERRORS IN THE STANDARD FBS FOR THE IP240.

ON AN EMERGENCY STOP, THE ”EMERG STOP” INDICATOR STAYS ON
AS LONG AS THE EMERGENCY OFF SWITCH IS DEPRESSED. OUTPUT OF AN ANALOG
VALUE IS BLOCKED, THE HEATER IS SWITCHED OFF, AND VARIOUS OUTPUTS AND FLAGS
ARE RESET.

ON A PARAMETER ASSIGNMENT ERROR THE CONTROLLER IS RESET.
THE ERROR FLAGS (FB11) ARE SAVED IN FB10 AND FB11 IS RESET.
THE ”FAULT” DISPLAY LAMP IS SWITCHED ON.

IF A LIMIT SWITCH IS ACTUATED, THE ”STOPPED” OUTPUT FLASHES
AS LONG AS THE SWITCH IS DEPRESSSED AND OUTPUT OF THE SPEED
IS PERMITTED IN THE OPPOSITE DIRECTION ONLY.


NAME :CHECK

0005      :A   I    4.0  -EMERG STOP
0006      :JC  =FOR1
0007      :S   Q   12.0  -STOPPED              INDICATOR
0008      :JU  =CHEK
0009 FOR1 :
000A      :R   Q   12.0  -STOPPED
000B      :L   FY  11                          PAFE BITS
000C      :L   KH 0000
000E      :OW
000F      :JZ  =FOR2                           BRANCH IF ZERO
0010      :T   FY  10    -CHEK BYTE       .    SAVE PAFE BITS
0011      :L   KB 0                           RESET PAFE BITS
0012      :T   FY  11
0013      :S   Q   12.5  -FAULT
0014      :JU  =CHEK
0015 FOR2 :
0016      :A   I    4.6  -LMTSW FORW          IF NO LIMIT SWITCH IS DEPRESSED,
0017      :A   I    4.7  -LMTSW BACK          END OF PROGRAM
0018      :JC  =END
0019      :
001A      :L   KT 025.0                       IF A LIMIT SWITCH IS REACHED,
001C      :AN  T    1                         OUTPUT ”STOPPED” SHOULD FLASH
001D      :SR  T    1                         FOR AS LONG AS THE SWITCH IS DEPRESSED
001E      :CU  C    1                         (0.5 SEC FREQUENCY)
001F      :L   C    1
0020      :T   FY   2    -AUX BYTE1
0021      :A   F    2.2                       WHEN COUNT IS 4,
0022      :R   C    1                         RESET COUNTER
0023      :
0024      :A   F    2.0                       O.5 SEC FREQUENCY
0025      :=   Q   12.0  -EMERG STOP
0026      :A   Q   12.4  -HEATING
0027      :R   Q   12.4  -HEATING              SWITCH OFF HEATING
0028      :AN  I    4.6  -LMTSW FORW
0029      :JC  =PRO1
002A      :AN  I    4.7  -LMTSW BACK
002B      :JC  =PRO2
002C PRO1 :
002D      :L   FW  14    -ANALOG VAL           IF UP COUNTING,
002E      :L   KB 0                           RESET OUTPUTS
002F      :>F
```

```
FB 26                                                    LEN=75

0030      :JC  =CHEK
0031      :JU  =END
0032 PRO2 :
0033      :L   FW  14    -ANALOG VAL           IF DOWN COUNTING,
0034      :L   KB 0                            RESET OUTPUTS
0035      :<F
0036      :JC  =CHEK
0037      :JU  =END
0038 CHEK:
0039      :R   Q   12.1  -RUNNING
003A      :R   Q   12.2  -ENABLED
003B      :S   Q   12.3  -RET INTPNT
003C      :R   Q   12.4  -HEATING
003D      :L   KB 0
003E      :T   FY  12                          AUXILIARY FLAGS
003F      :T   FW  14    -ANALOG VAL
0040 END  :
0041      :***

I    4.0 = EMERG STOP
Q   12.0 = STOPPED                 EMERG STOP PRESSED
FY  10   = CHECK BYTE              IMAGE OF FB11 IN CASE OF ERROR
Q   12.5 = FAULT                   FAULT FLAG FROM CONTROLLER (IP)
I    4.6 = LMTSW FORW              LIMIT SWITCH FURNACE FORWARD
I    4.7 = LMTSW BACK              LIMIT SWITCH FURNACE BACKWARD
FY   2   = AUX BYTE1               SCRATCH FLAG BYTE CYCLIC PROGRAM
Q   12.4 = HEATING                 HEATING ON (CONTACTOR + INDICATOR)
FW  14   = ANALOG VAL              ANALOG VALUE TO BE OUTPUT IN UNITS (MAX 1024)
Q   12.1 = RUNNING                 RUN STARTED
Q   12.2 = ENABLED                 NEW RUN POSSIBLE
Q   12.3 = RET INTPNT              INITIAL POINT MUST BE TRANSFERRED BEFORE RESTARTING

NETWORK 2      0042          OUTPUT OF SPEED
0042      :L   FW  14    -ANALOG VAL           ADAPTATION TO FORMAT OF
0043      :SLW      4                          THE ANALOG OUTPUT
0044      :T   PW 128                          ADDRESS OF ANALOG OUTPUT
0045      :BE

FW  14   = ANALOG VAL              ANALOG VALUE TO BE OUTPUT IN UNITS (MAX 1024)
```

```
FB 27                                                    LEN=26

NETWORK 1      0000          INTERRUPT SERVICE ROUTINE FOR THE IP 240

FB27 : INTERRUPT ORGANIZATION BLOCK FOR THE SAMPLE PROGRAM

INTERRUPT CAUSE/SOURCE IS DETERMINED AND THE APPROPRIATE INTERRUPT PROGRAM
(IN THIS CASE FB28) IS CALLED.

NAME :INTRT

0005      :JU  FB 170
0006 NAME :STEU.WEG
0007 DBNR :    KF +12
0008 FKT  :    KF +3                          READ INTERRUPT REQUEST BYTES
0009 PAFE :    FY   3    -AUX BYTE2
000A      :L   FY   3    -AUX BYTE2
000B      :L   KB 0
000C      :><F
000D      :=   F   11.3  -PAFE IR
000E      :A   DB  12
000F      :L   DW  20                          QUERY IF INTERRUPT WAS
0010      :L   KB 0                            GENERATED BY CHANNEL 1
0011      :><F
0012      :JC  FB  28                          INTERRUPT SERVICE ROUT. CHANNEL 1
0013 NAME :INTRT K1
0014      :BE

FY   3   = AUX BYTE2               SCRATCH FLAG BYTE INTERRUPT SERVICE ROUT.
F   11.3 = PAFE IR                 FOR READING INTERRUPT REQUEST BYTE (FB27)
```

```
FB 28                                                    LEN=81

NETWORK 1      0000          INTERRUPT SERVICE ROUTINE FOR THE IP 240 CHANNEL 1

FB28 : INTERRUPT SERVICE ROUTINE CHANNEL 1 OF THE IP240

PRECISE CAUSE OF INTERRUPT IS DETERMINED AND THE APPROPRIATE
RESPONSES ACTIVATED.

ON WIREBREAK OR REACHING ONE OF THE TWO FINAL POINTS (INITIAL POINT/TURNING POINT)
OF THE TRAVERSE PATH OF THE FURNACE, THE DRIVE IS SWITCHED OFF AND A FLAG
SET WHICH IS EVALUATED IN THE CYCLIC PROGRAM.

NAME :INTRT K1

0005      :C   DB  12
0006      :L   DR  29                        BITS FOR THE TRACKS USED (FROM
0007      :T   FY   3    -AUX BYTE2          FB24 CORRESPONDS TO THE ZONES USED)
0008      :
0009      :L   DW  20                        INTERRUPT REQUEST BYTE
000A      :T   FW  16    -AUX WORD4
000B      :L   KH 0004                       WIREBREAK?
000D      :AW
000E      :JN  =DRBR                         IF YES, WIREBREAK SERVICE ROUTINE
000F      :
0010      :C   DB  10
0011      :A   F   12.4  -BACK ACTIV
0012      :JC  =FOR2                         BACKWARD INTERRUPT SERVICE ROUTINE
0013      :A   F   12.2  -FORW ACTIV
0014      :JC  =FOR1                         FORWARD INTERRUPT SERVICE ROUTINE
0015      :BEU
0016 FOR1 :
0017      :AN  F   16.0                      REF1 (INITIAL ZONE 2)
0018      :ON  F    3.0                      BIT ZONE 2
0019      :JC  =REF2
001A      :L   DW   4                        SPEED IN ZONE 2
001B REF2 :
001C      :AN  F   16.1                      REF2 (INT.ZONE 3)
001D      :ON  F    3.1                      BIT ZONE 3
001E      :JC  =REF3
001F      :L   DW   5                        SPEED IN ZONE 3
0020 REF3 :
0021      :AN  F   16.2                      REF3 (INT.ZONE 4)
0022      :ON  F    3.2                      BIT ZONE 4
0023      :JC  =REF4
0024      :L   DW   6                        SPEED IN ZONE 4
0025 REF4 :
0026      :AN  F   16.3                      REF4 (INT.ZONE 5)
0027      :ON  F    3.3                      BIT ZONE 5
0028      :JC  =REF5
0029      :L   DW   7                        SPEED IN ZONE 5
002A REF5 :
002B      :AN  F   16.4                      REF5 (INT.ZONE 6)
002C      :ON  F    3.4                      BIT ZONE 6
002D      :JC  =REF6
002E      :L   DW   8                        SPEED IN ZONE 6
002F REF6 :
0030      :AN  F   16.5                      REF6 (INT.ZONE 7)
0031      :ON  F    3.5                      BIT ZONE 7
0032      :JC  =REF7
0033      :L   DW   9                        SPEED IN ZONE 7
0034 REF7 :
0035      :AN  F   16.6                      REF7 (INT.ZONE 8)
0036      :ON  F    3.6                      BIT ZONE 8
0037      :JC  =REF8
0038      :L   DW  10                        SPEED IN ZONE 8
```

```
FB 28                                                          LEN=81

0039 REF8 :
003A      :AN  F   16.7                       REF8 (CUTOFF POINT)
003B      :JC  =OUTP
003C      :S   F   12.6  -FIN POINT           BIT FOR FINAL POINT FORWARD REACHED
003D      :JU  =OUT1
003E FOR2 :
003F      :A   F   16.7                       REF8 (INITIAL POINT)
0040      :S   F   12.7  -INT POINT
0041      :JC  =OUT1
0042      :BEU
0043 DRBR :
0044      :S   F   11.7  -WIREBREAK
0045 OUT1 :
0046      :R   Q   12.4  -HEATING
0047      :L   KH 0000
0049 OUTP :
004A      :T   FW  14    -ANALOG VAL
004B      :BE

FY   3   = AUX BYTE2               SCRATCH FLAG BYTE INTERRUPT SERVICE ROUTINE
FW  16   = AUX WORD4               AUXILIARY FLAG WORD - INTERRUPT SERVICE ROUT.
                                   (STATUS BITS)
F   12.4 = BACK ACTIV              BACKWARD TRAVERSE PROGRAM ACTIVE
F   12.2 = FORW ACTIV              FORWARD TRAVERSE PROGRAM ACTIVE
F   12.6 = FIN POINT               FINAL POINT OF THE FORWARD TRAVERSE PROGRAM REACHED
F   12.7 = INT POINT               INITIAL POINT/ORIGINAL POSITION REACHED
F   11.7 = WIREBREAK               WIREBREAK/SHORT-CIRCUIT IN ENCODER   (FB28)
Q   12.4 = HEATING                 HEATING ON (CONTACTOR + INDICATOR)
FW  14   = ANALOG VAL              ANALOG VALUE TO BE OUTPUT IN UNITS  (UP TO 1024)
```

```
FB 38                                                          LEN=39

NETWORK 1      0000          SAVE FLAGS

FB38 SAVES FLAG WORDS 200 TO 254 IN A SPECIFIED DATA BLOCK.
THE DATA BLOCK MUST HAVE A LENGTH OF AT LEAST 30 DATA WORDS
(DW0 - DW29).

NAME :FLAG.SAV
ID   :DBNR      I/Q/D/B/T/C: B

0008      :B   =DBNR
0009      :***


NETWORK 2      000A
000A      :L   KF +200                        PRESET THE POINTERS
000C      :T   DW  29                         (DW28 AND DW29)
000D      :L   KF +0
000F      :T   DW  28
0010 M001 :DO  DW  29
0011      :L   MW   0
0012      :DO  DW  28
0013      :T   DW   0
0014      :L   DW  29                         INCREMENT THE POINTERS
0015      :ADD KF+2                           FLAG WORD POINTER
0017      :T   DW  29
0018      :L   DW  28
0019      :ADD KF+1                           DATA WORD POINTER
001B      :T   DW  28
001C      :L   KF +254                        FLAG WORDS 200 TO 254 SAVED
001E      :L   DW  29                         IN THE DATA BLOCK ?
001F      :>=F
0020      :JC  =M001
0021      :BE
```

```
FB 39                                                        LEN=37

NETWORK 1      0000          LOAD FLAGS

WRITE THE STATES OF FLAG WORDS 200 - 254 SAVED BACK TO
THE FLAG WORDS. THE DATA BLOCK SPECIFIED MUST HAVE A LENGTH OF
AT LEAST 30 DATA WORDS (DW0 - 29).

NAME :LOAD.FLG
ID   :DBNR      I/Q/D/B/T/C: B

0008      :B   =DBNR
0009      :***


NETWORK 2      000A
000A      :L   KF +0                          PRESET THE POINTERS
000C      :T   DW  28                         DATA WORD POINTER
000D      :L   KF +200
000F      :T   DW  29                         FLAG WORD POINTER
0010 M001 :DO  DW  28
0011      :L   DW   0
0012      :DO  DW  29
0013      :T   FW   0
0014      :L   DW  28                         INCREMENT POINTERS
0015      :ADD BF+1
0016      :T   DW  28
0017      :L   DW  29
0018      :ADD BF+2
0019      :T   DW  29
001A      :L   KF +254                        FLAG WORDS UP TO
001C      :L   DW  29                         AND INCLUDING FW254
001D      :>=F                                LOADED ?
001E      :JC  =M001
001F      :BE
```

```
FB 169                                                    LEN=47

NETWORK 1      0000
NAME :STRU.WEG
ID   :BGAD      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :KANR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :AFL       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :IMP       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DIG1      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KH
ID   :DIG2      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KH
ID   :PRA1      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KH
ID   :PRA2      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KH
ID   :PAFE      I/Q/D/B/T/C: A  BI/BY/W/D: BY
ID   :BER       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :ABIT      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KY

0029      :BE
```

```
FB 170                                                    LEN=20

NETWORK 1      0000
NAME :STEU.WEG
ID   :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :FKT       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :PAFE      I/Q/D/B/T/C: A  BI/BY/W/D: BY

000E      :BE
```

Figures

Tables

8 Counting

8.1 Applications

In this mode, the IP 240 can be universally used for pulse counting. The module can process pulse trains with frequencies of up to 70 kHz.

8.2 Principle of Operation

For the counting mode the following STEP 5 modules are necessary:

- A data block
  You must create a data block (DB) prior to calling the configuring function block for the first time. New data must be entered in this DB prior to its transfer to the IP 240 by the FB 172.
  Data that is read from the IP 240 is stored in this DB by control FB 172.
- Configuring FB 171
  You structure one or both channels of the IP 240 in position decoding mode with configuring FB 171. The configuring FB is normally called in the restart OB.
- Control FB 172
  The control FB 172 is called in the cyclic program or the interrupt program. By means of the FB parameter FKT you can specify whether data is to be read from or transferred to the IP 240.

8.2.1 Actual Value

Activating counting
Counting is activated with a positive-going edge of the gate signal. You can preset the gate signal with control bit **STRT** or via an external signal at input **GT**. On configuration, you must specify in parameter **EXT**, configuring FB 171, whether you are using STRT or GT as a gate signal.
If you use control bit STRT, you must first transfer the control bits with STRT=1 to the IP to form a positive-going gate edge. Set STRT bit D 17.4 to ”1” in the data block. Now call control FB 172 and initialize it for function 2 ”Writing control statements”. The CPU then transfers the control bits to the IP.

Generating the actual value
The pulses are counted on their positive-going edge while the gate signal is active. The counter counts down from an initial value **ANF**. After the actual value has crossed zero, the pulses are acquired with a negative sign if the gate signal is still active.

Counting range and overrange
The permissible counting range is defined from +9,999 to - 9,999. When the defined counting range is exceeded, the counter enters the overrange.

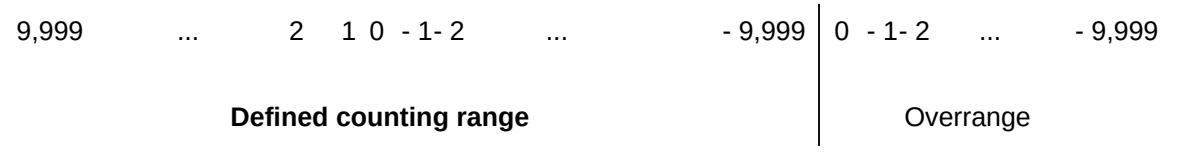


Fig. 8-1. Actual Value Range and Overrange in Counting Mode

When the defined actual value range is exceeded, the counter enters overrange and the IP sets status bit **UEBL (**overflow).
When set, the UEBL bit can trigger an interrupt. You must indicate whether or not it is to do so via the PRA parameter during configuring (Section 8.3.1). The UEBL bit is reset when the status area or interrupt request bytes are read.
When the counter has entered the overrange, the pulses are only counted. The next zero crossing does not generate another interrupt, and digital output D1 is not set.

Transferring a new initial value ANF to the IP
The first time an initial value is transferred to the IP, it is taken from the DB with configuring FB 171 and then displayed as an actual value.
You can, at any time, transfer a new initial value to the IP. It takes effect, however, only after termination of the current counting cycle when a positive-going edge occurs in the gate signal.

To transfer a new initial value, enter the new count value in data word 35 of the DB. Now call control FB 172 and initialize it for function 4 ”Write initial count”. The CPU then transfers the new initial value to the IP.

Reading the actual value
The actual value is updated on the IP in every module firmware cycle (the firmware is the IP 240's operating system).
For you to be able to read the current actual value from the DB, you must first call control FB 172 and initialize function 1 ”Reading the actual value, the final value and the status bits” (Section 8.3.2).

The CPU then transfers the current data from the IP to the data block. The data for the actual value are entered as follows:
- DW 31 Absolute actual value, in BCD code
- DW 33 Absolute actual value, in binary code
- D 19.0 Sign of the actual value (status bit SG)

After configuration, the initial value transferred is specified as actual value.

Monitoring actual value ”0”
If the actual value reaches ”0”, status bit **REF1** is set.

When set, REF1 can
- trigger an interrupt. You must indicate as much in the PRA parameter.
- set digital output D1. You must specify this option in the DIG parameter (Section 8.3.1).

At the start of a new counter, a positive gate signal edge resets REF1. If the count begins with ”0”, the first counting pulse sets REF1. Output D1 is not set.

8.2.2 Final Value

Storing the final count
When you evaluate the actual value, you are evaluating the current count. The IP also makes the actual value of the preceding count available, i.e. the count value at the instant of the first negative GATE signal. This is referred to as the final count. This value is retained until the next negative GATE signal, and can be read out from the IP.
When the final value is stored at termination of counting, status bit **REF2** is set.
When it is ”1”, REF2 can trigger an interrupt. You must specify this option in the PRA parameter during a configuring pass (Section 8.3.1).

REF2 is reset when the status area is read.

Reading the final value
Before you can read out the current final vaue from the DB, you must first invoke control FB 172 and initialize it for function ”1” Read actual value, final value and status bits”.
The CPU then transfers the current data from the IP to the data block. The data for the final value is entered as follows:
- DW 28 Absolute final value in binary
- D 27.0 Sign of the final value (SGF)

Overrange
If the actual value is already in the overrange at the instant of the negative GATE signal edge, status bit **UEBE** is set. UEBE is the overrange bit for the final value.

Overwriting an old final value
Every negative GATE signal edge overwrites the last final value with the new final value. If the status area (function 1, FB 172) was not read between two negative GATE edges, the **UEBS** bit is set on the IP. UEBS is the status bit for Overwrite.
When it is set, the UEBS bit can trigger an interrupt. You must specify this option in the PRA parameter.

Reading of the status area resets UEBS.

8.2.3 Forcing the IP Output

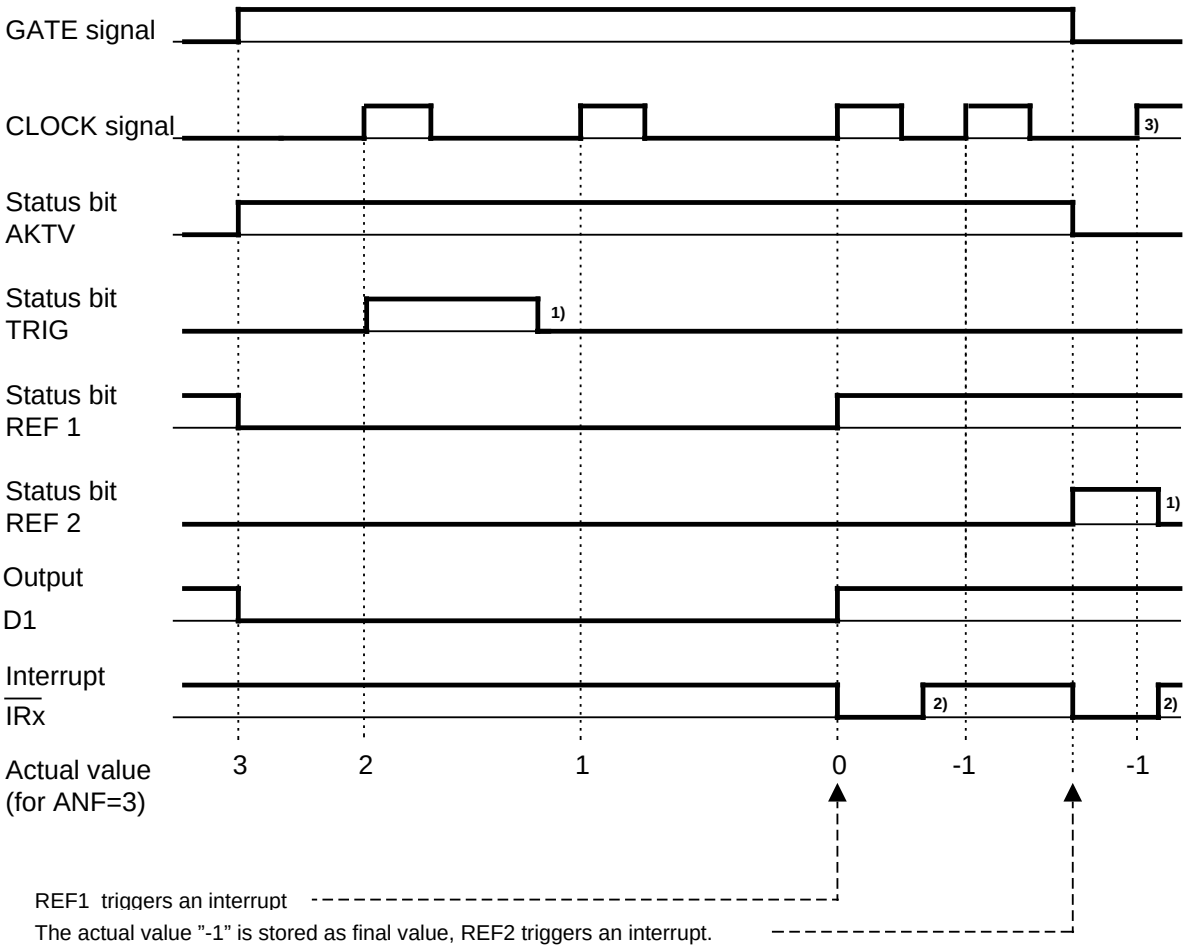
With control bits **DA1F** and **DA1S** in DL 17 you define how digital output **D1** is to be forced. Enter the required value in DL 17. Now call control FB 172 and initialize it for function 2 ”Write control statements”. The CPU then transfers the control bits to the IP.

The following options are available for forcing the output:

a) The digital output is to be set when the actual value reaches ”0”, and reset on the first positive GATE signal edge following the start of a new count.
   In this case, you must set control bits DA1F to 0 and DA1S to 1 in DL 17.
b) The digital output is to be reset without regard to the count.
   In this case, you must set control bits DA1F to 0 and DA1S to 0.
c) The digital output is to be set without regard to the count.
   In this case, you must set control bits DA1F to 1 and DA1S to 1.
   It is important to note that after transferring the control bits DA1f=1 and DA1s=1, the IP output D1 is to be reset by transferring the control bits DA1F=0 and DA1S=0, before the output control can be selected according to a) (DA1F=0 and DA1F=1)

Status bit **DA1** mirrors the current state of the output.

Figure 8-2 shows an example of triggering a process interrupt and activating the digital output.



1) These bits are reset on the IP following reading of the status area.
2) The interrupt request is reset when the interrupt request bytes are read.
3) This edge is no longer counted, as the GATE signal was set to ”0”.

Fig. 8-2. Sequence Diagram for Counting Mode

8.2.4 Flagging with Status Bits

Status data is updated in every cycle of the module firmware on the IP.
If you want information about the status, you must call control FB 172 and parameterize function 1 ”Read actual value, final value and status bits” (Section 8.3.2). The CPU then transfers the status bits from the IP to the data block (DW 18, 19 and 27).

Status bit **AKTV** (D 18.5) indicates whether the count has been enabled. It has the same meaning as a set gate signal.

Status bit **TRIG** (D 18.4) shows whether counting has begun. The status bit is set when after a positive-going gate edge the first pulse has been acquired. TRIG is reset when the status area is read again.

Status bit **DA1** (D 18.14) indicates whether digital output D1 is set.

Status bits for the actual value
Status bit **REF1** (D 19.8) indicates whether the count is less than or equal to zero. REF1 is set when the count reaches zero, and is reset with the next positive GATE signal edge.

Status bit **SG** (D 19.0) indicates whether the actual value stored in data words DW 31 and 33 is positive (SG=0) or negative (SG=1).

A ”1” value in statusbit **UEBL** (D 19.1) indicates that the actual value is out of range (actual value <-9,999). UEBL can trigger an interrupt. It is reset when
- the status area is read
- the interrupt request bytes are read if the overflow triggered the interrupt.

Status bits for the final value
Status bit **REF2** (D 19.9)=”1” indicates that the last count was terminated with the negative GATE signal edge and that the actual value was stored as final value of the count.

Status bit **SGF** (D 27.0) indicates whether the final value stored in data word DW 28 is positive (SGF=0) or negative (SGF=1).

When ”1”, status bit **UEBE** (D 27.1) indicates that the final value is out of range (final value <-9,999).

When ”1”, status bit **UEBS** (D27.2) indicates that an old final value was overwritten by a new final value although the old final value had not been read. UEBS can trigger an interrupt, and is reset when the status area is read.

> **Note**
>
> Once they have been read, status bits TRIG, UEBL, REF2 and UEBS, as well as all interrupt bits in the interrupt request bytes, are reset on the IP. The bits that were set can thus be read out only once.

8.2.5 Interrupt Generation and Processing

Status bits REF1, REF2, UEBL and UEBS can trigger an interrupt and are stored in the interrupt request bytes on the IP with their positive-going edges as RF1, RF2, UEB and UBS (Section 8.3.3).

Reading the interrupt request bytes
After an interrupt request, an interrupt service organization block is called by the CPU. You must call a control FB in this interrupt OB and parameterize ”Read interrupt request bytes” with FCT=3. The control FB transfers the interrupt request bytes of both channels to the specified DB (DW 20 and 21). By evaluating these bytes in the interrupt service OB, you can react in a way appropriate to the cause of the interrupt.

Reading these bytes has the following effect:
- the bits in the interrupt request bytes on the IP are reset
- the interrupt request is withdrawn by the IP
- status bit UEBL is reset if this was the error which caused the interrupt.

As the interrupt request bytes are read across all channels, the current status can only be read once from the IP and only the DB parameterized in the control FB can be directly updated.

Masking the interrupts
You can mask all bits with interrupt capability in the relevant channel by setting control bit **AMSK** (D 17.15). Masked interrupts do not result in an interrupt request and are not stored in the interrupt request bytes, i.e. they are lost.

Calling the interrupt service OBs in the S5-150U and S5-155U (150 mode)
In the S5-150U and S5-155U (150 mode), the relevant interrupt service OB is called at the next block boundary on a signal change in a bit in PY 0. Using the parameter ABIT in configuring FB 171 (Section 8.3.1) you can specify whether the interrupt service OB is to be called on every change or only on a change from 0 to 1.

Setting the ABIT parameter:

ABIT : KY x,y
- x>0 : the interrupt OB is called on every signal transition.
- x=0, y=0 to 7 : the interrupt OB is called only on a signal transition from 0 to 1.
  y must be set to the number of the bit in I/O byte 0 which you set on switchbank S1 (Section 5.1.2).

Note

Please observe the description of the encoder signals and the timing requirements for counting mode presented in Chapter 13.
Detailed information on response times is presented in Chapter 12.

8.3 Initializing Standard Function Blocks and Data Block Contents

8.3.1 Configuring Function Block

FB 171 (STRU.DOS) Configuring and parameter assignments for operation of the IP 240 in counting mode

Functional description

The configuring function block first checks the parameter assignments and then transfers the general module data (machine-readable product code of the module, firmware and hardware versions) from the IP to the data block specified. It then verifies its compatibility with the firmware and transfers the error flags of the start check (Section 6.3) to the data block.

The configuring data (parameter entries in FB 171) and initial count value are then transferred from the DB to the IP 240.

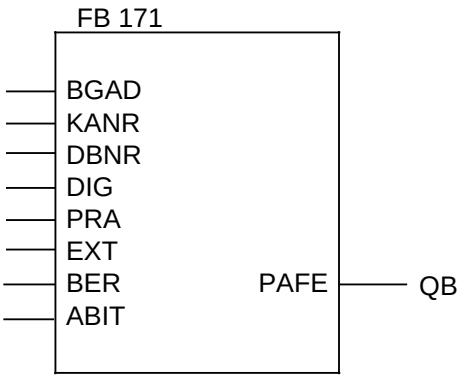
After error-free configuring of the specified channel, the identifier of the configured mode is entered in DW 23.

If the IP 240 is reconfigured, active outputs are reset and any process interrupts for the channel are cancelled.

Hardware, communications and parameter assignment errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. In the event of an error, the relevant channel is not configured.

Function block call

The configuring function block is usually called in the restart organization blocks.

STL	LAD/CSF
: JU FB 171 NAME : STRU. DOS BGAD : KF KANR : KF DBNR : KF DIG : KH PRA : KM EXT : KH PAFE : QB BER : KF ABIT : KY	

Note

Specification of the address space (BER) is dispensed with for the function block for the S5-115U programmable controller (normal I/O area only, Chapter 3).

The ABIT parameter is not required in the function blocks for the S5-115U and S5-135U.

Table 8-1. Parameters for Configuring FB 171

Name	Para-meter type	Data	Description
BGAD	D	KF	Module starting address
KANR	D	KF	Channel number
DBNR	D	KF	Data block number
DIG	D	KH	Assignment of digital output D1
PRA	D	KM	Assignment of process interrupt
EXT	D	KH	Control of count enabling
PAFE	Q	BY	Error flag byte
BER*	D	KF	Address space (normal and extended I/O areas)
ABIT**	D	KY	Evaluation of the signal transition for interrupt processing with I/O byte 0. Interrupt bit assigned in I/O byte 0.

* not for FB 171 for the S5-115U

** not for FB 171 for the S5-115U and S5-135U

Parameter assignments

BGAD: KF 128-240 Starting address of module in the I/O area, (P area) divisible by 16

0-240 Starting address of module in the extended I/O area (Q area), divisible by 16

KANR: KF 1 Channel 1

2 Channel 2

DBNR: KF 3-255 Number of the data block created

DIG : KH 0000 -0001 Assignment of digital output D1

Bit 0=1 Output D1 is set when reference bit REF1 goes to ”1” and reset on a positive GATE signal edge.

Bit 0=0 Output D1 is not set when reference bit REF1 goes to ”1”.

PRA : KM 0000 0000 - 00001111 Assignment of process interrupts

Bit 0=1 An interrupt is generated when reference bit REF1 goes to ”1” (count has reached ”0”).

Bit 0=0 No interrupt is generated when reference bit REF1 goes to ”1”.

Bit 1=1 An interrupt is generated when status bit UEBL goes to ”1” (actual value out of range).

Bit 1=0 No interrupt is generated when status bit UEBL goes to ”1”.

Bit 2=1 An interrupt is generated when reference bit REF2 goes to ”1” (final value stored).

Bit 2=0 No interrupt is generated when reference bit REF2 goes to ”1”.

Bit 3=1 An interrupt is generated when status bit UEBS goes to ”1” (final value overwritten).

Bit 3=0 No interrupt is generated when status bit UEBS goes to ”1”.

EXT : KH 0000 to 0001 Control of count enabling by external or internal starting signal

Bit 0=1 Control of start of count by active signal at GT input
Bit 0=0 Control of start of count by active control bit STRT

PAFE : QB Flag byte or output byte (0 to 239) in which any errors are flagged
(Section 6.4)

BER : KF 0 Addressing in the I/O area (P area)
1 Addressing in the extended I/O area (Q area)

ABIT : KY x,y **x**=0 to 255 x>0 : the interrupt service OB is called on every change in the interrupt bit

x=0 : the interrupt service OB is called only when the interrupt bit goes from 0 to 1

y=0 to 7 the interrupt bit assigned in I/O byte 0 as set on switchbank S1

Note

Interrupt servicing is not disabled in the configuring FBs. You must therefore ensure the noninterruptibility of the configuring FBs in the S5-115U and S5-135U (when interrupt servicing after each statement has been specified) and in the S5-155U (155U mode) by writing the STEP 5 program accordingly. Interrupt servicing is already disabled in the restart OBs.

The effects of configuring on the cycle time
Because of the increase in the module firmware's cycle time for configuring of a channel, the STEP 5 program must be written in such a way that the other channel is in a safe wait state while a configuring FB is executing.

Technical Specifications

Block number : 171

Block name : STRU. DOS

PLC	Library number	Call length/ Block length	CPU	Processing time [1]
S5-115U	P71200-S 5171-D-2	9 words/ 814 words	941-7UA...	approx. 72 ms
			942-7UA...	approx. 46 ms
			943-7UA...	approx. 30 ms
			944-7UA...	approx. 13 ms
			941-7UB...	approx. 27 ms
			942-7UB...	
			943-7UB...	
			944-7UB...	approx. 11.5
S5-135U/ S5-135U	P71200-S 9171-D-2	10 words/ 1248 words	922 from A9	approx. 25 ms
			928-3UA...	approx. 18 ms
			928-3UB...	approx. 11 ms
S5-150U	P71200-S 4171-D-1	11 words/ 1256 words		approx. 12 ms
S5-155U	P71200-S 6171-B-1	11 words/ 1302 words	946-3UA.../ 947-3UA...	approx. 11 ms

Nesting depth : 0

Subordinate blocks : none

Assignments in data area : data block specified with DBNR parameter up to and including DW 35

Assignments in flag area : MB 240 to 255

System statements : yes

[1] The specified processing times are for an FB call following an IP 240 firmware cycle without data interchange.

8.3.2 Control Function Block

FB 172 (STEU.DOS) Control function block for counting.

Functional description
The control function block first verifies whether the addressed channel has been configured for counting mode. Depending on the parameters assigned to the function block, certain data areas are transferred from the data block to the IP 240, or updated in the DB by reading them from the IP 240.

The following functions are possible:
- Reading the actual value, final value and status bits
- Writing the control statements (control bits)
- Reading the interrupt request bytes
- Writing the initial count value

Communications and parameter assignment errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. The specified function is not executed in the event of an error.

Function block call
The control FB is usually called in the cyclic program and in the interrupt service organization blocks.

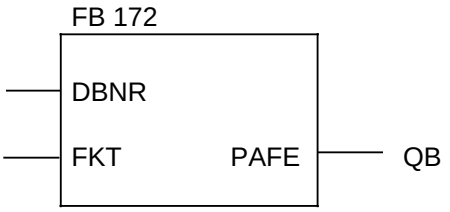
STL	LAD/CSF
: JU FB 172 NAME: STEU.DOS DBNR: KF FKT : KF PAFE : QB	

Table 8-2. Parameters for Control FB 172

Name	Parameter type	Data type	Description
DBNR	D	KF	Data block number
FKT	D	KF	Function number
PAFE	Q	BY	Error identifier byte

Parameter assignments

DBNR: KF 3 - 255 Number of the data block created

FKT : KF
- 1 Read actual value, final value and status bits
- 2 Write control statements (control bits)
- 3 Read interrupt request bytes
- 4 Write initial count value

PAFE : QB Flag byte or output bytes (0 to 239) in which any errors are flagged (Section 6.4)

Note

In the standard function blocks, scratch flags and system data areas are used for data interchange with the IP 240 (Technical Specifications for the FBs).
You must

- save these scratch flags and data areas at the beginning of the interrupt service routines for the S5-115U and S5-135U (when interrupt servicing after each statement is enabled) and for the S5-155U (155U mode) and reload them at the end of these routines.
- save these flags and data areas in the restart routines for manual or automatic restart (OB21/OB22) in the S5-135U (basic setting for restart mode) and S5-150U and reload them at the end of these routines.

Technical Specifications

Block number : 172
Block name : STEU. DOS

PLC	Library number	Call length/ Block length	CPU	Processing time Function [1]				
S5-115U	P71200-S 5172-D-2	5 words / 680 words	941-7UA...	approx.	38	18	24	24 ms
			942-7UA...	approx.	20	10.5	13	13 ms
			943-7UA...	approx.	12.5	6.2	8.2	7.0 ms
			944-7UA...	approx.	2.8	2.5	2.6	2.7 ms
			941-7UB... / 942-7UB... / 943-7UB...	approx.	11	6.0	7.4	6.0 ms
			944-7UB...	approx.	2.1	1.6	1.9	2.2 ms
S5-135U/ S5-155U	P71200-S 9172-D-2	5 words/ 1110 Worte	922 from A9	approx.	10	6.0	7.6	7.0 ms
			928-3UA...	approx.	6.0	3.5	4.2	4.2 ms
			928-3UB...	approx.	2.2	1.8	1.9	2.0 ms
S5-150U	P71200-S 4172-D-1	5 words/ 1054 words		approx.	1.9	1.2	1.4	1.6 ms
S5-155U	P71200-S 6172-B-1	5 words/ 1311 words	946-3UA.../ 947-3UA...	approx.	2.2	1.6	2.0	1.8 ms

Nesting depth : 0
Subordinate blocks : S5-115U OB160 (only CPUs ...-7UB...)
S5-135U OB122
S5-155U OB91, OB122
Assignments in data area : data block specified with DBNR parameter up to and including DW 35
Assignments in flag area : MB 240 to 255
System statements : yes

[1] The specified processing times are for an FB call following an IP 240 firmware cycle without data interchange. Note that

- following reading out of data from the IP 240, no further data interchange is possible in the current cycle.
- following the writing of new data to the IP 240, no further data interchange is possible in the current or in the next cycle.

8.3.3 Contents of the Data Block

The data block to be created must have least 36 words (DW0 to DW 35). The number of the selected data block must be entered under parameter DBNR when calling an FB.

DW 0	
DW 1 DW 2 DW 3	**Machine-readable product code of module**
DW 4 DW 5 DW 6	**Version of the module firmware**
DW 7	**Version of the module hardware**
DW 8 DW 9 DW 10	**Error messages for hardware and communications errors**
DW 11 DW 12	
DW 13	**Error message for parameter assignment errors**
DW 14 DW 15 DW 16	
DW 17	**Control bits**
DW 18 DW 19	**Status bits**
DW 20 DW 21	**Interrupt request bytes for Channel 1** **Interrupt request bytes for Channel 2**
DW 22	
DW 23	**Bits for configured mode and DB number**
DW 24 DW 25 DW 26	
DW 27 DW 28	**Status bits for final value** **Final value in binary**

DW 29	
DW 30 DW 31	**Actual value in BCD**
DW 32 DW 33	**Actual value in binary**
DW 34 DW 35	**Initial count**

This data can be transferred from the DB to the IP 240 and must be adapted in the DB beforehand.

If you wish to read the current values in the appropriate data areas, you must call the control FB and parameterize Read function 1 or 3.

This data is specified by the parameters assigned to the configuring FB or is transferred from the IP 240 to the DB when the module is configured.

These data words are used internally, and may not be modified.

Control bits

Data byte	Bit 7	6	5	4	3	2	1	0
DL 17	AMSK	0	0	0	0	0	DA1F	DA1S
DR 17	0	0	0	STRT	0	0	0	0

AMSK =1 All process interrupts for the channel are masked, i.e. lost
=0 Process interrupts enabled

DA1F DA1S
0 0 Digital output D1 is reset
0 1 Digital output D1 is set and reset on a mode-dependent basis
1 1 Digital output D1 is set irrespective of the actual value

STRT =1 Enable a count (effective only
=0 Stop a count when EXT=0)

Status bits

Data byte	Bit 7	6	5	4	3	2	1	0
DL 18	0	DA1	0	0	0	0	0	0
DR 18	0	0	AKTV	TRIG	0	0	0	0
DL 19	0	0	0	0	0	0	REF2	REF1
DR 19	0	0	0	0	0	0	UEBL	SG

DA1 =1 Digital output D1 is set
=0 Digital output D1 is not set

AKTV =1 Count has been enabled
=0 Count has not been enabled

TRIG =1 Counting has started (first counting pulse acquired)

REF1 =1 Actual value has reached ”0”
=0 Actual value has not yet reached ”0”

REF2 =1 The last count was terminated with a negative GATE edge and the final value stored

UEBL =1 Negative actual value range violation (actual value < - 9, 999)

SG =1 Actual value specified in DW 31 and DW 33 is negative
=0 Actual value specified in DW 31 and DW 33 is positive

Interrupt request bytes for channel 1 and channel 2

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 20	0	0	0	0	0	0	RF 2	RF 1	Channel 1
DR 20	0	0	0	0	0	UBS	0	UEB	Channel 1
DL 21	0	0	0	0	0	0	RF2	RF1	Channel 2
DR 21	0	0	0	0	0	UBS	0	UEB	Channel 2

RF1 =1 Process interrupt was triggered by a positive-going edge of reference bit REF1 ("0" reached)

RF2 =1 Process interrupt was triggered by a positive-going edge of reference bit REF2 (last count terminated and final value stored)

UEB =1 Process interrupt was triggered by a positive-going edge of status bit UEBL (count out of range)

UBS =1 Process interrupt was triggered by a positive-going edge UEBS (last count terminated and final value stored)

Bits for the configured mode and data block number

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 23	0	0	0	0	0	0	1	0	
DR 23	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DB No.

After error-free configuring of the channel, a bit combination corresponding to the mode is entered in DL 23.

DL 23=02_H Channel has been configured for counting mode
DR 23= No. of the data block, in binary, specified during configuring

Status bits for the final value and final value in binary

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 27	0	0	0	0	0	0	0	0	
DR 27	0	0	0	0	0	UEBS	UEBE	SGF	
DL 28	0	0	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	Final
DR 28	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	value

SGF =1 The final value specified in DW 28 is negative
=0 The final value specified in DW 28 is positive

UEBE =1 Actual value exceeds negative range (final value < - 9 999)

UEBS =1 Old value was overwritten without being read

DW 28 : Final value in binary; the specified value is the absolute final value

Actual value
The specified value is an absolute value. The **sign (SG)** is indicated in the status area (DW 19).

Actual value in BCD

Data byte	Bit 7	6	5	4	3	2	1	0
DL 30	0	0	0	0	0	0	0	0
DR 30	0	0	0	0	0	0	0	0
DL 31	10^3				10^2			
DR 31	10^1				10^0			

Actual value in binary

Data byte	Bit 7	6	5	4	3	2	1	0
DL 32	0	0	0	0	0	0	0	0
DR 32	0	0	0	0	0	0	0	0
DL 33	0	0	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
DR 33	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Initial count (ANF)

Data byte	Bit 7	6	5	4	3	2	1	0
DL 34	0	0	0	0	0	0	0	0
DR 34	0	0	0	0	0	0	0	0
DL 35	10^3				10^2			
DR 35	10^1				10^0			

Permissible range: 0 to 9,999

8.4 Example for Counting: Fast Filling with Loose Material

The throughput in filling with loose material is measured using a pulse encoder. This encoder drives the counter on the IP 240 directly.
When the specified setpoint is reached, the valve is closed by the IP 240 hardware.

- Digital output 1 of the first channel on the IP 240 closes an auxiliary relay.
- The auxiliary relay's NC contact is connected in series to a normal CPU digital output (Q4.0).

Starting with the valve closed, the procedure is as follows:

1. The user enters the required amount of loose material in DW 34/35 (initial count value) of the DB 14.
2. When the pushbutton ”START FILL” (I 5.3) is pressed, the proportioning procedure is activated, shown by the ”FILLING” indicator (Q4.1).
3. When 0 is reached, the IP 240 closes on the auxiliary relay, thus opening the output ”OPEN VALVE” (Q.4.0). The valve can close.
4. The state of the counter is only read after a delay (5 s) so that the valve has time to close properly before the final count is read by the IP. The value is then kept in DD 30 or DD 32 of DB 14 until a new proportioning procedure is activated.
5. When the ”FILLING” indicator goes out, filling can be reactivated by pressing ”START FILL”.

A proportioning procedure can only be interrupted by pressing ”EMERG STOP”. If filling is to be resumed where it was interrupted, the actual value in DB 14 must be entered in DD 34 as the initial count value and ”START FILL” pressed. Otherwise filling would start from the beginning when ”START FILL” is pressed. As long as ”EMERG STOP” is pressed, the ”FILLING” indicator flashes slowly.
If ”FILLING” flashes fast, this indicates a parameter assignment error in the STEP 5 program. The system can only be restarted after a PLC cold restart or by resetting the ”GROUPPAFE” flag (F 11.0) reset.

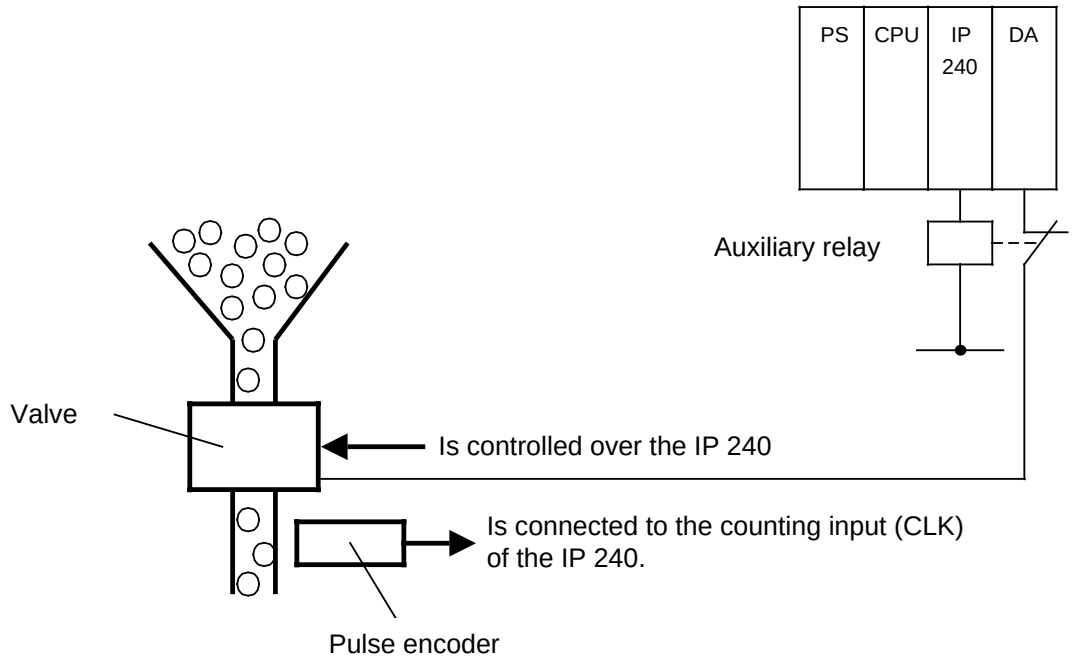


Fig. 8-3. Diagrammatic Representation of the Example ”Fast Filling with Loose Material”

Inputs, outputs, flags, timers and counters used

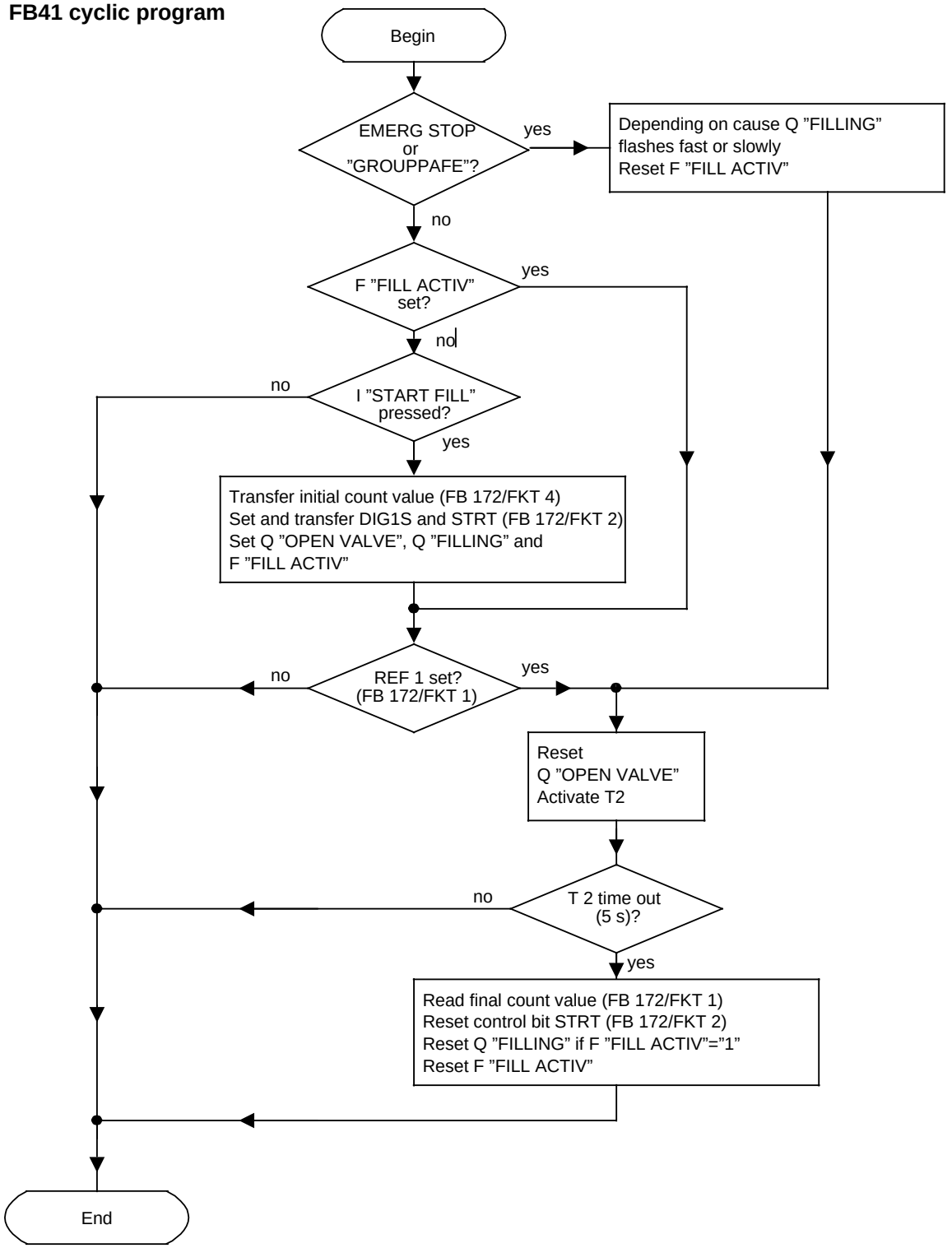
```
OPERAND    SYMBOL        COMMENT

I  5.2      EMERG STOP
I  5.3     START FILL    PUSHBUTTON TO ACTIVATE PROPORTIONING PROCEDURE

Q 4.0      OPEN VALVE    OUTPUT TO OPEN THE VALVE
Q  4.1     FILLING       INDICATOR, LIT DURING PROPORTIONING

FY 8       AUX BYTE      SCRATCH FLAG BYTE IN IP240 PROGRAM
F 10.0     FILL ACTIV    AUX FLAG: PROPORTIONING PROCEDURE STARTED
F 11.0     GROUPPAFE     GROUP SIGNAL FROM ALL FB171/172

T 1        BLINKER       )  TO GENERATE FLASHING FREQUENCY
C 1        CONVERT       )

T 2        DELAY         DELAY UNTIL VALVE IS CLOSED
```

```
DB14                                                    LEN=43

 0:     KH = 0000;
 1:     KS ='      ';                    MACHINE-READABLE PRODUCT CODE OF THE MODULE
 4:     S  ='      ';                    FIRMWARE VERSION
 7:     KS ='  ';                        HARDWARE VERSION
 8:     KH = 0000;                       ERROR FLAGS FOR
 9:     KH = 0000;                       HARDWARE AND
10:     KH = 0000;                       COMMUNICATIONS ERRORS
11:     KH = 8001;
12:     KH = 0000;
13:     KH = 0000;                       PAFE BITS
14:     KH = 0001;
15:     KH = 0000;
16:     KH = 0008;
17:     KM = 0000000100010000;           CONTROL BITS
18:     KM = 0000000000100000;           STATUS BITS
19:     KM = 0000000000000000;           STATUS BITS
20:     KM = 0000000000000000;           INTERRUPT REQUEST BYTES CHANNEL1
21:     KM = 0000000000000000;           INTERRUPT REQUEST BYTES CHANNEL2
22:     KH = 0000;
23:     KY = 002,014;                    MODE AND DB NUMBER
24:     KH = 0000;
25:     KH = 0000;
26:     KH = 0000;
27:     KH = 0000;
28:     KH = 0000;
29:     KH = 0000;
30:     KH = 0000;                   ACTUAL VALUE IN BCD CODE
31:     KH = 0030;
32:     KM = 0000000000000000;       ACTUAL VALUE IN BINARY CODE
33:     KM = 0000000000011110;
34:     KH = 0000;                   INITIAL COUNT VALUE
35:     KH = 0040;
36:     KS ='END';                   FREE FOR USER FROM DW36 ON
38:
```

```
DB20                                                LEN=35

 0:     KH = 0000;
 1:     KH = 0000;
 2:     KH = 0000;
 3:     KH = 0000;
 4:     KH = 0000;
 5:     KH = 0000;
 6:     KH = 0000;
 7:     KH = 0000;
 8:     KH = 0000;
 9:     KH = 0000;
10:     KH = 0000;
11:     KH = 0000;
12:     KH = 0000;
13:     KH = 0000;
14:     KH = 0000;
15:     KH = 0000;
16:     KH = 0000;
17:     KH = 0000;
18:     KH = 0000;
19:     KH = 0000;
20:     KH = 0000;
21:     KH = 0000;
22:     KH = 0000;
23:     KH = 0000;
24:     KH = 0000;
25:     KH = 0000;
26:     KH = 0000;
27:     KH = 0000;
28:     KF = +00000;                    DATA WORD POINTER
29:     KF = +00000;                    FLAG WORD POINTER
30:
```

FB 40 initialization program

FB41 cyclic program



```
OB 1                                                        LEN=8

NETWORK 1    0000          CYCLE
0000      :JU FB  41
0001 NAME :IP PROG
0002      :BE



OB 20    (For S5-115U: OB 21)
                                                            LEN=9

NETWORK 1     0000         COLD RESTART
0000      :
0001      :JU FB  40                        CONFIGURING THE IP 240
0002 NAME :CONFIG
0003      :BE



OB 22                                                       LEN=17

NETWORK 1    0000          WARM RESTART AFTER POWER OFF
0000      :
0001      :JU FB  38                        SAVE SCRATCHPAD FLAGS (FB200-255)
0002 NAME :FLAG.SAV
0003 DBNR :    DB  20
0004      :
0005      :JU FB  40                        CONFIGURING THE IP 240
0006 NAME :CONFIG
0007      :
0008      :JU FB  39                        RELOAD SCRATCH FLAGS
0009 NAME :LOAD FLG
000A DBNR :    DB  20
000B      :BE
```

FB 38 and FB 39 are not required in the S5-115U or S5-155U, or in the S5-135U when ”automatic cold restart after power on” is set in DX0.

```
FB 38                                                          LAE=39

NETWORK 1     0000          SAVE FLAGS

FB 38 SAVES FLAG WORDS 200 TO 254 TO A SPECIFIED DATA BLOCK.
THE DATA BLOCK MUST COMPRISE AT LEAST 30 DATA WORDS (DW0 TO DW29).

NAME :FLAG.SAV
BEZ  :DBNR      I/Q/D/B/T/C: B

0008      :B   =DBNR
0009      :***


NETWORK 2     000A
000A      :L   KF +200                        INITIALIZE THE POINTERS
000C      :T   DW  29                         (DW28 AND DW29)
000D      :L   KF +0
000F      :T   DW  28
0010 M001 :B   DW  29
0011      :L   MW   0
0012      :B   DW  28
0013      :T   DW   0
0014      :L   DW  29                         INCREMENT THE POINTERS
0015      :ADD KF +2                          FLAG WORD POINTER
0017      :T   DW  29
0018      :L   DW  28
0019      :ADD KF +1                          DATA WORD POINTER
001B      :T   DW  28
001C      :L   KF +254                        FLAG WORDS 200 TO 254
001E      :L   DW  29                         SAVED IN DATA BLOCK ?
001F      :>=F
0020      :JC  =M001
0021      :BE
```

```
FB 39                                                        LEN=37

NETWORK 1     0000          WRITE FLAGS

FB39 WRITES THE STATES OF FLAG WORDS 200 TO 254 SAVED WITH FB 38 BACK
TO THE FLAG WORDS. THE DATA BLOCK SPECIFIED MUST COMPRISE AT LEAST 30 DATA WORDS
(DW0 TO DW29).
NAME :LOAD FLG
BEZ  :DBNR      I/Q/D/B/T/C: B

0008      :B   =DBNR
0009      :***


NETWORK 2     000A
000A      :L   KF +0                          INITIALIZE THE POINTERS
000C      :T   DW  28                         DATA WORD POINTER
000D      :L   KF +200
000F      :T   DW  29                         FLAG WORD POINTER
0010 M001 :DO  DW  28
0011      :L   DW   0
0012      :DO  DW  29
0013      :T   FW   0
0014      :L   DW  28                         INCREMENT THE POINTERS
0015      :ADD BF +1
0016      :T   DW  28
0017      :L   DW  29
0018      :ADD BF +2
0019      :T   DW  29
001A      :L   KF +254                        ALL FLAG WORDS UP TO
001C      :L   DW  29                         AND INCLUDING FW254
001D      :>=F                                RELOADED ?
001E      :JC =M001
001F      :BE
```

```
FB 40                                                    LEN=31

NETWORK 1     0000          CONFIGURING THE IP240 CHANNEL 1


CHANNEL 1 OF THE IP 240 IS CONFIGURED IN COUNTING MODE.
DIGITAL OUTPUT 1 AND THE INTERNAL GATE CONTROL ARE ENABLED.
THE CONTROL BITS ARE ALSO INITIALIZED AND TRANSFERRED.


NAME :CONFIG

0005      :JU FB 171
0006 NAME :STRU.DOS
0007 BGAD :    KF +128                        MODULE ADDRESS OF THE IP 240
0008 KANR :    KF +1                          CHANNEL NUMBER
0009 DBNR :    KF +14                         DATA BLOCK 14 => CHANNEL 1
000A DIG  :    KH 0001                        ENABLE THE DIGITAL OUTPUT
000B PRA  :    KH 0000                        NO PROCESS INTERRUPTS
000C EXT  :    KH 0000                        INTERNAL GATE CONTROL
000D PAFE :    FY   8    -AUX BYTE            ERROR BYTE
000E BER  :    KF +0                          I/O AND E I/O AREA (NOT FOR 115U)
000F ABIT :    KY 1,0                         SYSTEM DATA RS0 IS NOT
0010      :                                   AFFECTED WHEN
0011      :                                   FB172/FCT3 IS INVOKED (ONLY FOR 150U)
0012      :L   KB 0
0013      :L   FY   8    -AUX BYTE            SCAN FOR ERROR FLAG
0014      :><F
0015      :S   F   11.0  -GROUPPAFE           GROUP SIGNAL FOR PAFE
0016      :
0017      :A   F   10.0  -FILL ACTIV          RESET AUXILIARY FLAGS
0018      :R   F   10.0  -FILL ACTIV
0019      :BE

FY   8   = AUX BYTE                SCRATCH FLAG BYTE IN THE IP 240 PROGRAM
F   11.0 = GROUPPAFE                GROUP SIGNAL FROM ALL FB171/172
F   10.0 = FILL ACTIV               AUX. FLAG: PROPORTIONING STARTED
```

```
FB 41                                                        LEN=111

NETWORK 1     0000          ORGANIZATION BLOCK FOR CHANNEL1


FB41 CONTAINS THE PROGRAM FOR CHANNEL 1 OF THE IP 240 IN COUNTING MODE.

NAME :IP PROG

0005      :AN  F   11.0  -GROUPPAFE
0006      :A   I    5.2  -EMERG STOP
0007      :JC =CYCL
0008      :R   F   10.0  -FILL-ACTIV          RESET THE AUXILIARY FLAGS
0009      :AN  T    1    -BLINK               GENERATE FLASHING
000A      :L   KT 005.0                       OF 0.5 HZ FOR EMERG OFF
000C      :SR  T    1    -BLINK               INDICATOR AND ROUTE TO
000D      :CU  C    1    -CONVERT             ”FILLING” INDICATOR
000E      :L   C    1    -CONVERT
000F      :T   FY   8    -AUX BYTE
0010      :A   F    8.4
0011      :R   C    1    -CONVERT
0012      :A   F    8.3
0013      :AN  I    5.2  -EMERG STOP
0014      :O
0015      :A   F    8.1
0016      :A   F   11.0  -GROUPPAFE
0017      :=   Q    4.1  -FILLLING
0018      :JU =OFFP
0019 CYCL :A   F   10.0  -FILL ACTIV
001A      :JC =SCAN
001B      :AN  I    5.3  -START FILL
001C      :R   Q    4.1  -FILLING
001D      :JC =END
001E      :JU FB 172                          START OF FILLING PROCEDURE
001F NAME :STEU.DOS
0020 DBNR :    KF +14
0021 FKT  :    KF +4                          TRANSFER INITIAL COUNT
0022 PAFE :    FY   8    -AUX BYTE
0023      :L   KB 0
0024      :L   FY   8    -AUX BYTE
0025      :><F
0026      :S   F   11.0  -GROUPPAFE
0027      :A   DB  14
0028      :L   KH 0110                        SET DIG1S AND STRT
002A      :T   DW  17
002B      :JU  FB 172
002C NAME :STEU.DOS
002D DBNR :    KF +14
002E FKT  :    KF +2                          TRANSFER CONTROL STATEMENT
002F PAFE :    FY   8    -AUX BYTE
0030      :L   KB 0
0031      :L   FY   8    -AUX BYTE
0032      :><F
0033      :S   F   11.0  -GROUPPAFE
0034      :UN  F   10.0  -FILL ACTIV
0035      :S   F   10.0  -FILL ACTIV
0036      :S   Q    4.0  -OPEN VALVE
0037      :S   Q    4.1  -FILLING
0038 SCAN :                                   SCAN FOR ZERO CROSSING
0039      :JU  FB 172
003A NAME :STEU.DOS
003B DBNR :    KF +14
003C FKT  :    KF +1                          READ ACTUAL VAUE AND STATUS BITS
003D PAFE :    FY   8    -AUX BYTE
003E      :L   KB 0
```

```
FB 41                                                        LEN=111

003F      :L   FY   8    -AUX BYTE
0040      :><F
0041      :S   F   11.0  -GROUPPAFE
0042      :C   DB  14
0043      :L   DL  19                          REF1
0044      :L   KB 1
0045      :AW
0046      :JZ  =END
0047 OFFP :A   Q    4.0  -OPEN VALVE           SWITCHOFF PROGRAM AND READING
0048      :R   Q    4.0  -OPEN VALVE           FINAL COUNT VALUE AFTER 5 SEC
0049      :L   KT 050.1
004B      :SE  T    2    -DELAY
004C      :A   T    2    -DELAY
004D      :JC  =END
004E      :A   T    2    -DELAY               ACTIVATE TIMER 2 WITH RLO 0
004F      :SE  T    2    -DELAY               TO RESET IT
0050      :JU  FB 172
0051 NAME :STEU.DOS
0052 DBNR :    KF +14
0053 FKT  :    KF +1                          READ ACTUAL VALUE AND STATUS BITS
0054 PAFE :    FY   8    -AUX BYTE
0055      :L   KB 0
0056      :L   FY   8    -AUX BYTE
0057      :><F
0058      :S   F   11.0  -GROUPPAFE
0059      :C   DB  14
005A      :L   KH 0100                       RESET CONTROL BIT STRT
005C      :T   DW  17                        (DIG1S REMAINS "1")
005D      :JU  FB 172
005E NAME :STEU.DOS
005F DBNR :    KF +14
0060 FKT  :    KF +2                          TRANSFER CONTROL STATEMENTS
0061 PAFE :    FB   8    -AUX BYTE
0062      :L   KB 0
0063      :L   FY   8    -AUX BYTE
0064      :><F
0065      :S   F   11.0  -GROUPPAFE
0066      :A   F   10.0  -FILL ACTIV
0067      :R   Q    4.1  -FILLING
0068      :R   F   10.0  -FILL ACTIV
0069 END  :BE

F   11.0 = GROUPPAFE              GROUP SIGNAL FROM ALL FB171/172
I    5.2 = EMERG STOP
F   10.0 = FILL ACTIV             AUXILIARY FLAG: PROPORTIONING STARTED
T    1   = BLINK                  ) FOR GENERATING A BLINK FREQUENCY
C    1   = CONVERT                )
FY   8   = AUX BYTE               SCRATCH FLAG BYTE IN IP240 PROGRAM
Q    4.1 = FILLING                INDICATOR, LIT DURING PROPORTIONING
I    5.3 = FILL START             PUSHBUTTON TO ACTIVATE PROPORTIONING
Q    4.0 = OPEN VALVE             OUTPUT FOR OPENING THE VALVE
T    2   = DELAY                  DELAY UNTIL VALVE IS CLOSED
```

```
FB 171                                                    LEN=38

NETWORK 1     0000
NAME :STRU.DOS
BEZ  :BGAD      I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :KANR      I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :DIG       I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KH
BEZ  :PRA       I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KH
BEZ  :EXT       I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KH
BEZ  :PAFE      I/Q/D/B/T/C: A  BI/BY/W/D: BY
BEZ  :BER       I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :ABIT      I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KY

0020      :BE
```

```
FB 172                                                    LEN=20

NETWORK 1     0000
NAME :STEU.DOS
BEZ  :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :FKT       I/Q/D/B/T/C: D  KM/KH/KY/KC/KF/KT/KS/KG: KF
BEZ  :PAFE      I/Q/D/B/T/C: A  BI/BY/W/D: BY

000E      :BE
```

Figures

Tables

9 IP 252 Expansion

When the IP 240 is used with the IP 252 closed-loop control module, control lines, which are only implemented in the S5-115U programmable controller with a PS 7A/15A power supply, are required to coordinate direct data exchange between the modules.
The following explanations for this special mode therefore relate only to the S5-115U programmable controller.

9.1 Speed Measurement with the IP 252; DRS Controller Structure

The IP 252 high-speed closed-loop control module has eight separate control loops which can be provided with actual values via their own analog inputs. Only one input is provided on the module for connecting incremental encoders.

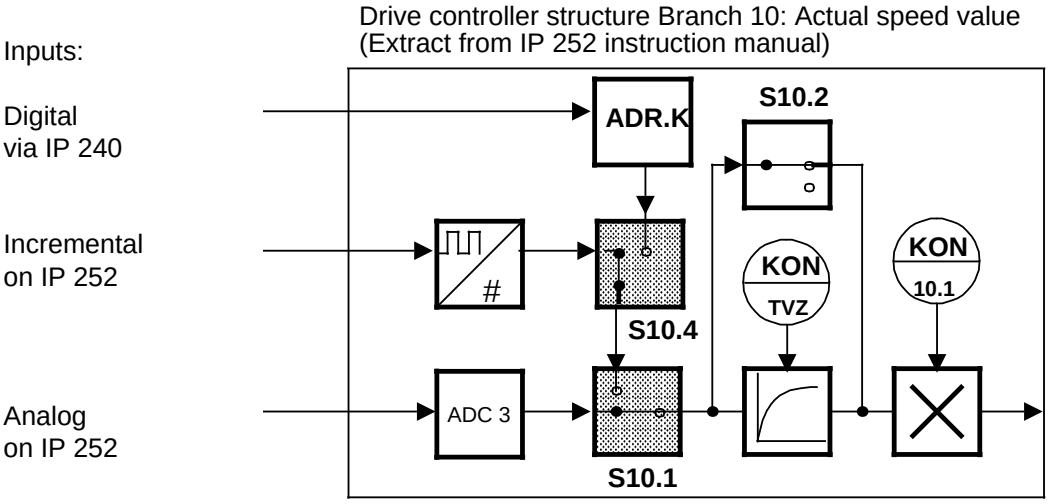


Fig. 9-1. Speed Measurement with the IP 252 Closed-Loop Control Module

Note

The IP 240 can only be connected to the IP 252
- if an IP 252 with machine-readable product code 6ES5-3AA13, version A04 or newer, is used,
- if the IP 252 is equipped with an 6ES5 374-0AB11 submodule,
- if the COM REG IP 252 software package beginning release A05 or COM REG GRAPHIC IP 252 is used.

If you are using a CPU 944, you require MLFB 6ES5 944-7UA12 or -7UA22 or newer.

By expanding the IP 252 with IP 240 modules, it is possible to provide two or more control loops with actual values from incremental encoders.
In these cases, the IP 240 operates as a slave module for the IP 252.

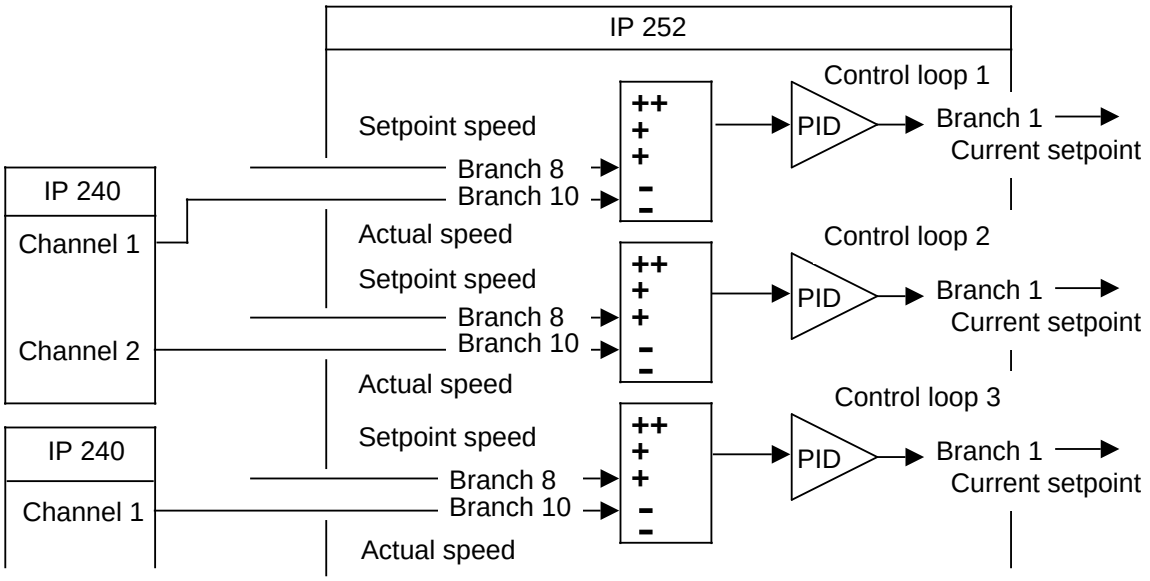


Fig. 9-2. Actual Speed Measurement via the IP 240 Module

Note

If two or more IP 252 closed-loop control modules are used in one central controller, both channels on an IP 240 must be assigned to the same IP 252. An IP 240 cannot be accessed by more than one IP 252.
Each channel of an IP 240 can provide only one control loop with data.

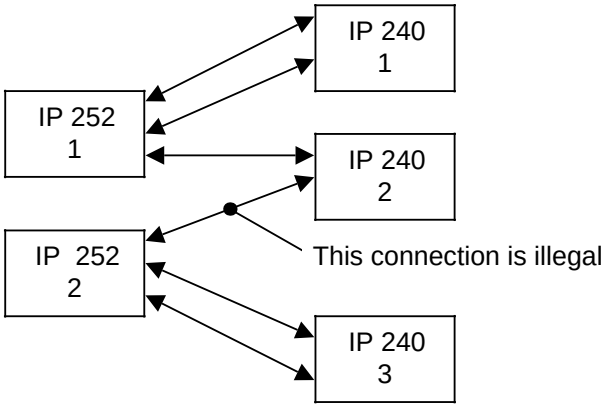


Fig. 9-3. Assignment of IP 240 Modules to IP 252 Modules

9.2 Data Interchange between S5 CPU -- IP 240 -- IP 252

During operation, data traffic between the IP 240 and the IP 252 is controlled by the closed-loop control module. CPU access to the backplane bus is prevented during the data interchange.

The following data is stored by the IP 240, on request, in a transfer buffer on the IP 240 which can be read by the IP 252:

- Direction on rotation
- Count
- Interval since the last count
- Wirebreak/short-circuit in the lines of encoders with symmetrical pulse trains.

The **closed-loop control module** computes the actual speed from the data transferred.

CPU access to the IP 240 is not possible during operation. No control function block is therefore available.

Configuring of the IP 240 takes place as for the other modes during execution of restart blocks OB21 and OB22.

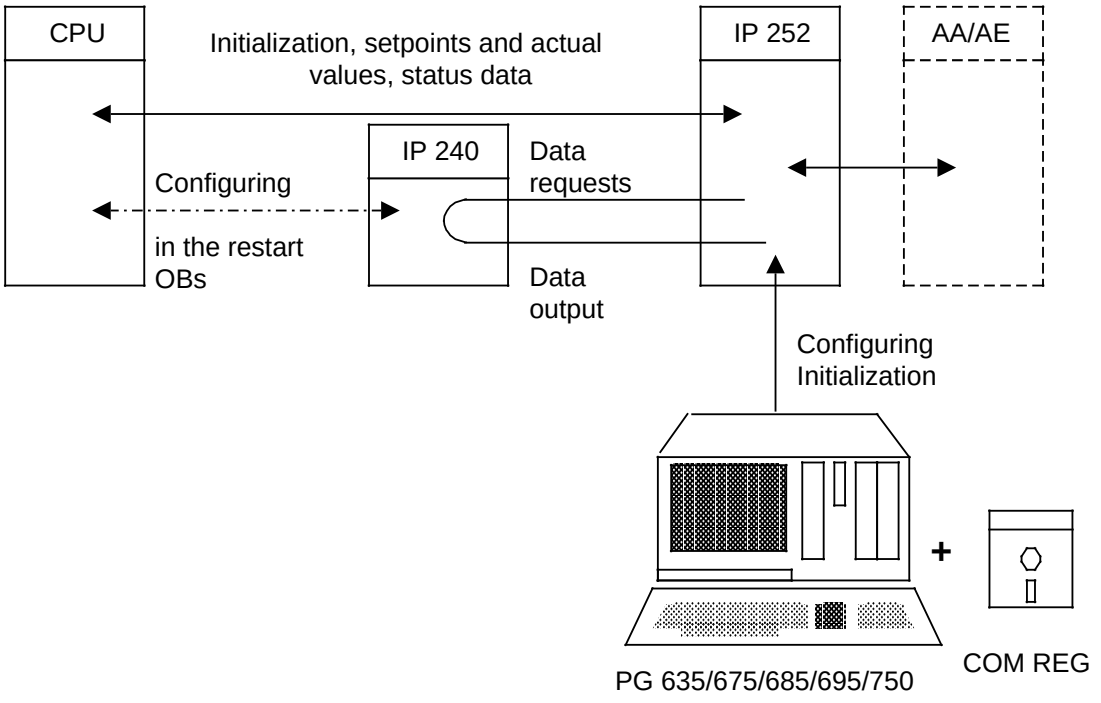


Fig. 9-4. Data Interchange between S5 CPU - IP 240 - IP 252

> **Note**
>
> The digital outputs of the IP 240 cannot be driven in IP 252 expansion mode.

9.3 Configuring

When configuring the IP 252 closed-loop control module, you must set the configuring switches — for speed measurement so that the actual count is interrogated by the IP 240. Furthermore, during initialization the I/O address and the assigned channel of the IP 240 must also be specified.

The IP 240 is configured by calling function block FB 173 in restart organization blocks OB21 and OB22. In this mode, both channels are configured simultaneously; a second mode on the IP 240 is therefore not possible.

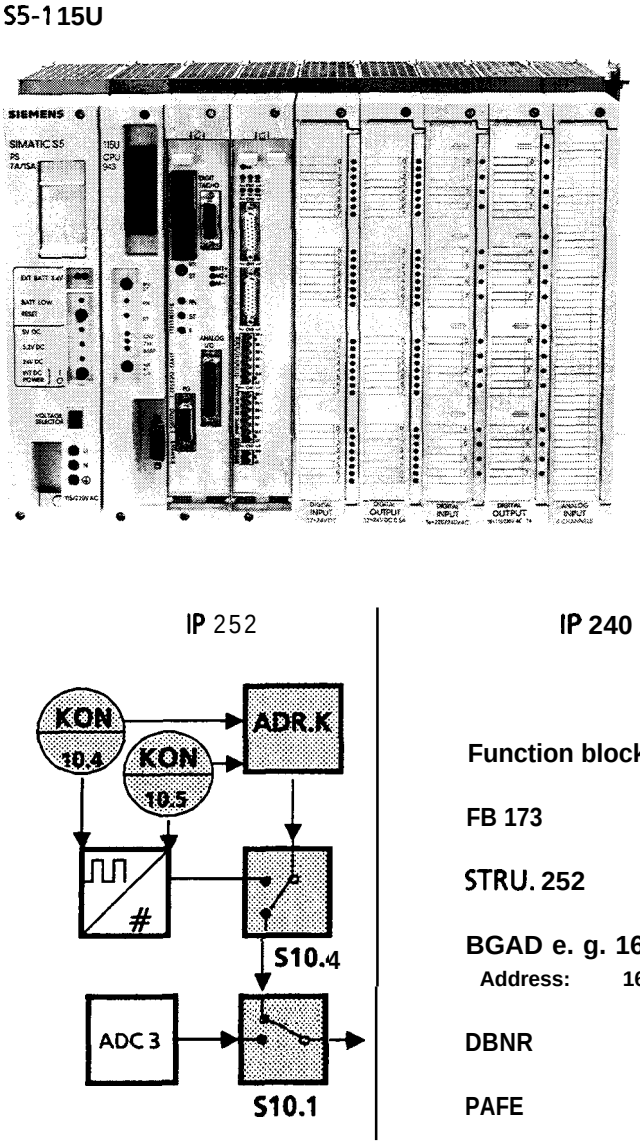


Fig. 9-5. Configuring the Modules

Note

In IP 252 expansion mode, the input signals are processed as for position decoding. See Chapter 13 for information on encoder signals and Section 7.2.1 for information on the direction of rotation (direction of counting).

9.4 Initializing the Configuring Function Block and Data Block Contents

9.4.1 Configuring Function Block

FB 173 (STRU. 252) Configuring the module in the IP 252 expansion mode

Functional description
The configuring function block first checks the parameters and then transfers the general module data (machine-readable product code of the module, firmware and hardware version) from the IP to the specified data block. It then checks its compatibility with the firmware version and transfers the error flags from the restart check (Section 6.3) to the data block.
The configuring data (parameter entries in FB 173) are then transferred to the IP.
After error-free configuration and parameter assignment, the identifier of the configured mode is entered in DW 23.
Hardware, communications and parameter assignment errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. If an error is detected, the module is not configured.

Function block call
The configuring function block is usually called in the restart organization blocks.

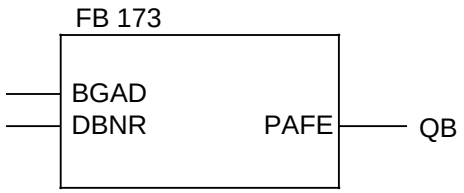
STL	LAD/CSF
: JU FB 173 NAME : STRU. 252 BGAD : KF DBNR : KF PAFE : QB	

Table 9-1. Parameters of Configuring FB 173

Name	Parameter type	Data type	Description
BGAD	D	KF	Module starting address
DBNR	D	KF	Data block number
PAFE	Q	BY	Error byte

Parameter assignments

BGAD : KF 128 to 240 Starting address of the module in the I/O area, divisible by 16

DBNR : KF 3 to255 Number of the data block created

PAFE : QB Flag byte or output byte (0 to 239) in which any errors are flagged (Section 6.4)

Note

Interrupt servicing is not disabled in the configuring FBs. You must therefore write your STEP 5 program in such a way that the configuring FB cannot be interrupted. Interrupt servicing is disabled in the restart OBs.

Technical Specifications

Block number : 173

Block name : STRU. 252

AG	Library number	Call length/ Block length	CPU	Processing time[1]
S5-115U	P71200-S 5173-D-2	5 words/ 562 words	941-7UA...	approx. 64 ms
			942-7UA...	approx. 45 ms
			943-7UA...	approx. 30 ms
			944-7UA...	approx. 17 ms
			941-7UB...	approx. 29 ms
			942-7UB...	
			943-7UB...	
			944-7UB...	approx. 16 ms

Nesting depth : 0

Subordinate blocks : none

Assignment in data area : at data block specified with DBNR parameter up to and including DW 24

Assignment in flag area : MB 240 to 255

System statements: yes

[1] The specified processing times are for an FB call following an IP 240 firmware cycle without data interchange.

9.4.2 Data Block Contents

The data block to be created must have at least 25 words (DW 0=to DW 24). The number of the selected data block must be entered under parameter DBNR when the FB is called.

DW 0	
DW 1 DW 2 DW 3	**Machine-readable product code of the module**
DW 4 DW 5 DW 6	**Version of the module firmware**
DW 7	**Version of the module hardware**
DW 8 DW 9 DW 10	**Error messages for hardware and communications errors**
DW 11 DW 12	
DW 13	**Error message for parameter assignment errors**

DW 14 DW 15 DW 16 DW 17 DW 18 DW 19 DW 20 DW 21 DW 22	
DW 23	**Identifier of the configured mode and DB no.**
DW 24	

This data is specified by the parameters assigned to the configuring FB or transferred from the IP 240 to the DB when configuring the module.

These data words are used internally and may not be modified.

Identifier of the configured mode and DB no.

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 23	0	0	0	0	0	0	1	1	
DR 23	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DBNR

After error-free configuring of the module, a bit combination corresponding to the mode is entered in DL 23.

DL 23 = 03_H	Both channels have been configured in the IP 252 expansion mode
DR 23	Number of the data block, in binary, specified during configuring

Figures

Tables

10 Positioning

10.1 Application and Functional Description

10.1.1 Application

In this mode, the IP 240 enables controlled positioning with cut-off points.
Incremental encoders must be used to generate the path-dependent signals. To acquire the encoder signals, the IP 240 is equipped with counter chips which can process encoder signal trains of up to 500 kHz from symmetrical encoders and of up to 50 kHz from asymmetrical encoders. To evaluate the encoder signals, the IP 240 compares the computed actual value with the specified setpoints in every module firmware cycle (the firmware is the IP 240's operating system) and initiates the programmed reactions.
The various configuring and synchronization options make it possible to use the IP 240:

- for positioning tasks in which the IP 240 controls the positioning drive (e.g. control of handling units etc.)
- for control tasks in which actual value-dependent post-processing steps are required (e.g. labeling etc.) and
- for gate-controlled counting of encoder pulses (e.g. length measurement etc.).

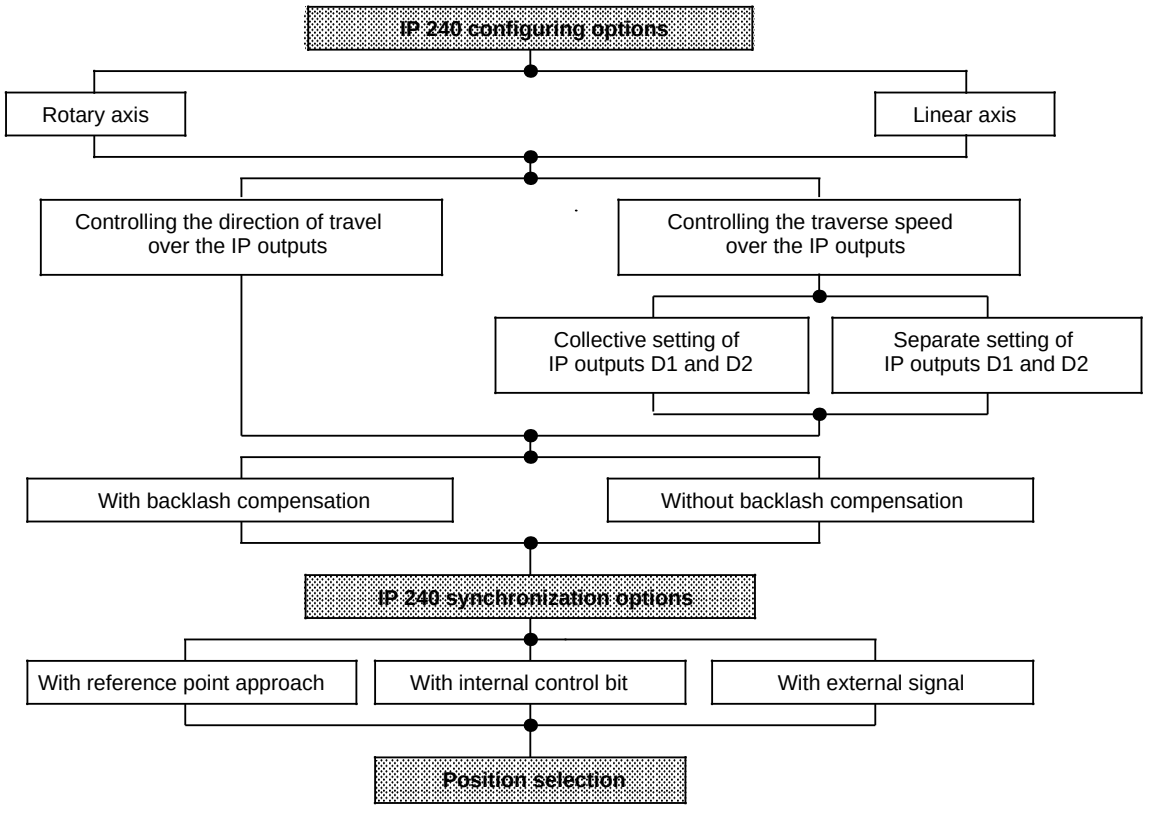


Fig. 10-1. Overview of IP 240 Configuring and Synchronization Options

10.1.2 Functional Description

This section includes a brief description of the IP 240's method of operation in ”positioning” mode and provides explanations of terms used in subsequent sections.

Configuring the IP, data interchange
The IP 240 is a two-channel module. You can configure one or both channels for ”positioning” mode using configuring function block FB 167. The configuring FB is invoked in the restart organization blocks.
After configuring, you can initiate data interchange between the S5 CPU and the IP 240 to read the actual value, the status bits and the interrupt bits, and to specify the new position using control function block FB 168. For special applications, you can also program direct data interchange yourself.
Both standard function blocks require a data block for data interchange. You must generate the data block prior to the first FB call.

Controlled positioning
For controlled positioning, the approach to the position is defined on a time-dependent or path-dependent basis. When the cut-off point is reached, the positioning drive is stopped and the actual value is no longer corrected. Fig. 10-2 illustrates a typical positioning sequence with a motor designed for two speeds:
- Switch on motor, rapid traverse
- Switch to creep speed
- Switch off motor.

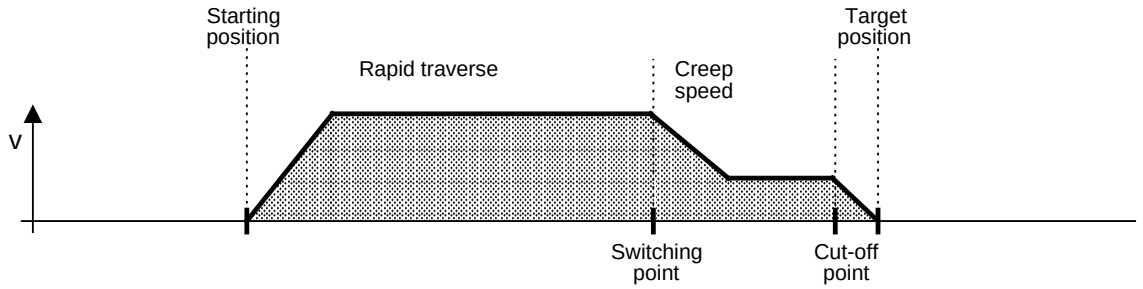


Fig. 10-2. Controlled Positioning with Two Speeds

Controlled positioning with the IP 240
In order to control this positioning sequence with the IP 240, the module requires:
- An incremental encoder for generating the path-dependent signals,
- Synchronization of the actual value,
- The position value of the target position and
- The distance of the switching point and the cut-off point from the position value.

The synchronization of the actual value determines the zero point (reference point) of the actual value range. The actual value and the position values relate to this point.

Because the positions can be approached from both directions, the IP 240 computes range BEE1 from the distance of the switching point and range BEE2 from the distance of the cut-off point (Fig. 10-3). The module firmware compares these ranges with the computed actual value. Depending on the result of the setpoint/actual-value comparison:
- Status bits are set and reset,
- Outputs are switched and
- Interrupts are generated on the IP 240.

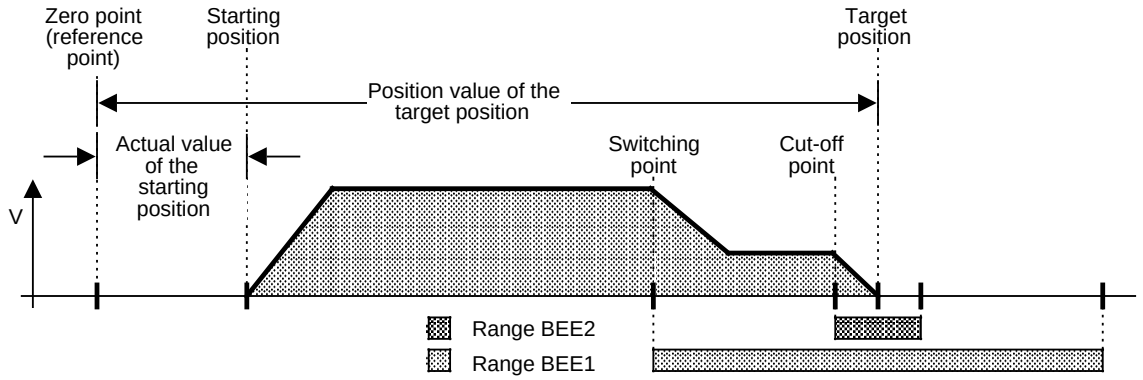


Fig. 10-3. Controlled Positioning with the IP 240

The IP 240's module firmware can control the traverse speed and the direction of travel directly over the IP's two digital outputs. For positioning with two speeds and from two directions, one of the two functions must be initiated by the IP 240 via status or interrupt signals and controlled via the S5 CPU over two auxiliary digital outputs.

Table 10-1. Switching IP Digital Outputs D1 and D2

• Output active	IP controls the speed Variant 1		IP controls the speed Variant 2		IP controls the speed	
	Rapid traverse	Creep speed	Rapid traverse	Creep speed	Positive direction	Negative direction
IP output D1	•		•		•	
IP output D2		•	•	•		•

Configuring and approaching a position

a) Position number and position value

You can store up to 254 positions per channel on the IP 240. Each position has a position number and a position value. You invoke a stored position over the position numer (one byte) and identify the location of the target position in the traverse range over the position value.

To avoid on-loading cyclic operation with additional interchanging of data, the position numbers and the associated position values are initially transferred to the IP 240 when the channel is configured. You can change the position values after configuring.

b) Switching and signalling ranges for a position
During the approach to a target position, the IP 240 monitors the entry into ranges BEE1 and BEE2 in order to be able to control the drive. Overtravel and standstill of the axis after the drive has been switched off, however, must also be considered. You can define a target range (BEE3) for this purpose. The IP 240 signals entry into and exiting of this range via status bits and interrupts.
You must define all three ranges over their distance to the position value. The resulting ranges are symmetrical to the target position.

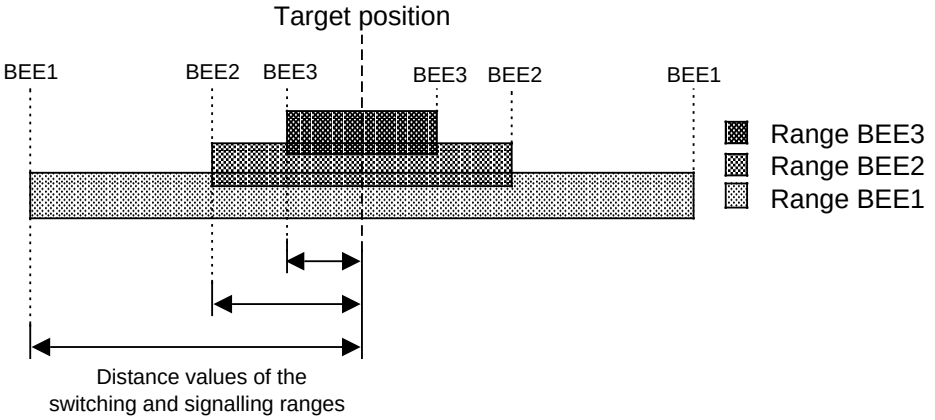


Fig. 10-4. Setting up a Position

The specified distance values apply for all positions stored on the IP 240. The following must be observed when defining the distance values:
Distance value to range BEE1 distance value to range BEE2 distance value to range BEE3.

c) Approaching a position
To invoke one of the positions 1 to 254 you need only forward the position number to the IP 240. The IP takes the value stored under this position number as the new position value and updates the status bits in accordance with the current actual value.
Each of the BEE ranges (1, 2 and 3) is assigned a status bit, which is
- set to ”1” when the actual value is out of range and
- set to ”0” when the actual value is in range or at a range limit.

The direction bit (RICH) indicates the direction in which the actual value must be modified in order to reach the target position.
- If RICH=0, traverse must be in a positive direction (ascending actual value).
- If RICH=1, traverse must be in a negative direction (descending actual value).

Note that both IP outputs must be disabled when a position between 1 and 254 is selected. Once the position has been selected, the outputs are set in dependence on the actual value.

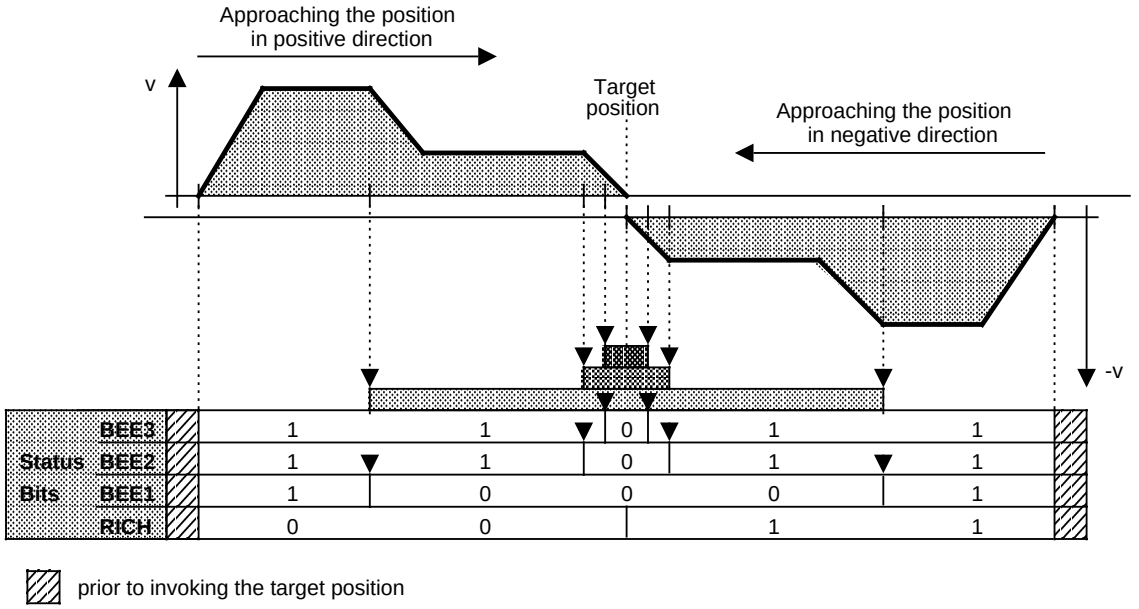


Fig. 10-5. Status Bits on Approach to Position

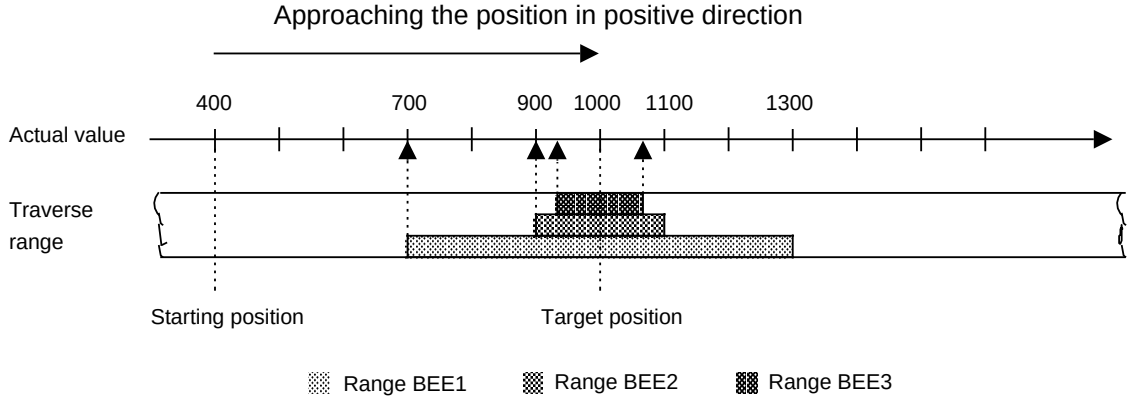
Example: The examples below will help you understand positioning from a positive and from a negative direction:

Position data for the target position to be approached:

Position value for the target position:	1000 increments
Distance value to range BEE1:	300 increments
Distance value to range BEE2:	100 increments
Distance value to range BEE3:	70 increments

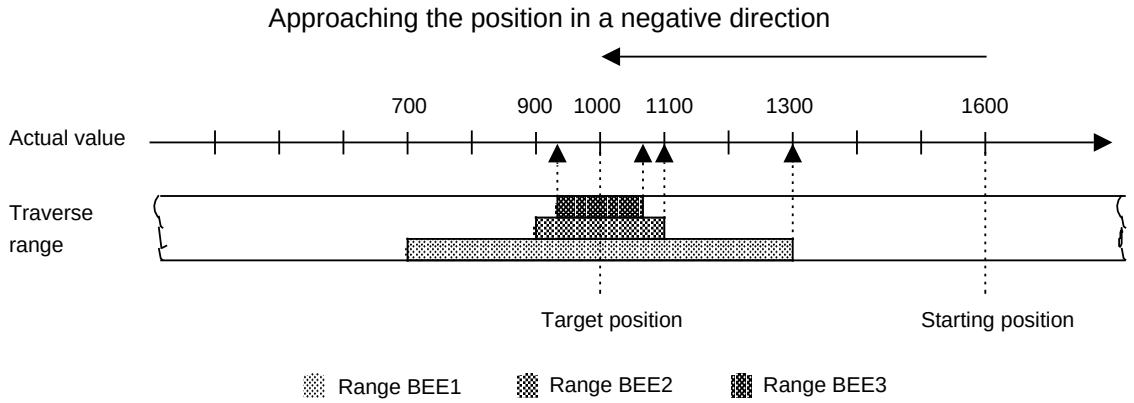
a) Approaching the target position in positive direction. When the position is selected, the axis is at 400 increments. The axis must travel in a positive direction at the rapid traverse rate.
- When the actual value is 700, the traverse rate is switched to creep speed.
- When the actual value is 900, the drive is switched off.
- When the actual value is 930, the target position has been reached.

The IP 240 monitors the actual value range 930 to 1070, and signals exiting of this target range without a new position having been selected.



b) Approaching the target position in negative direction
The axis is at 1600 increments when the position is selected. The axis must travel in the negative direction at the rapid traverse rate.
- When the actual value is 1300, the traverse rate is switched to creep speed.
- When the actual value is 1100, the drive is switched off.
- When the actual value is 1070, the target range has been reached.

The IP 240 monitors the actual value range 1070 to 930, and signals exiting of this target range without a new position having been selected.



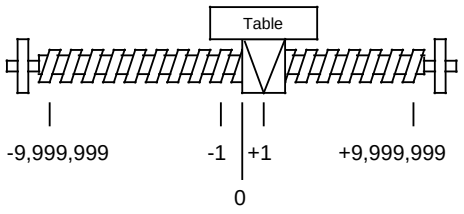
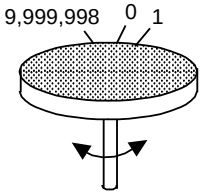
Position 0
In addition to positions 1 to 254, you can also use position 0.
Position 0 is not stored on the IP 240. To define this position, you must transfer the new position value to the IP 240. This position can also be selected when the channel's IP outputs are still set. This allows you to intervene in a positioning process that is already in progress.
When position 0 is selected, the IP 240 immediately takes the new position value as setpoint and updates the status bits and the states of the outputs.

Table 10-2. Selecting Positions 0 - 254

Position	Is selected by	Note
0	Transferring the position value	This postion can also be selected when the IP outputs are set.
1 to 254	Transferring the position number	These positions may be selected only when the IP outputs are disabled.

Axis types and actual value ranges
You can operate the IP 240 with a linear axis (limited traverse range) and a rotary axis (rotary table, endless conveyor belt). The required axis type is specified during configuring.

Table 10-3. Axis Types and Actual Value Ranges

Axis types	Linear axis	Rotary axis
		
Maximum actual value	-9,999,999 to +9,999,999	0 to 9,999,998

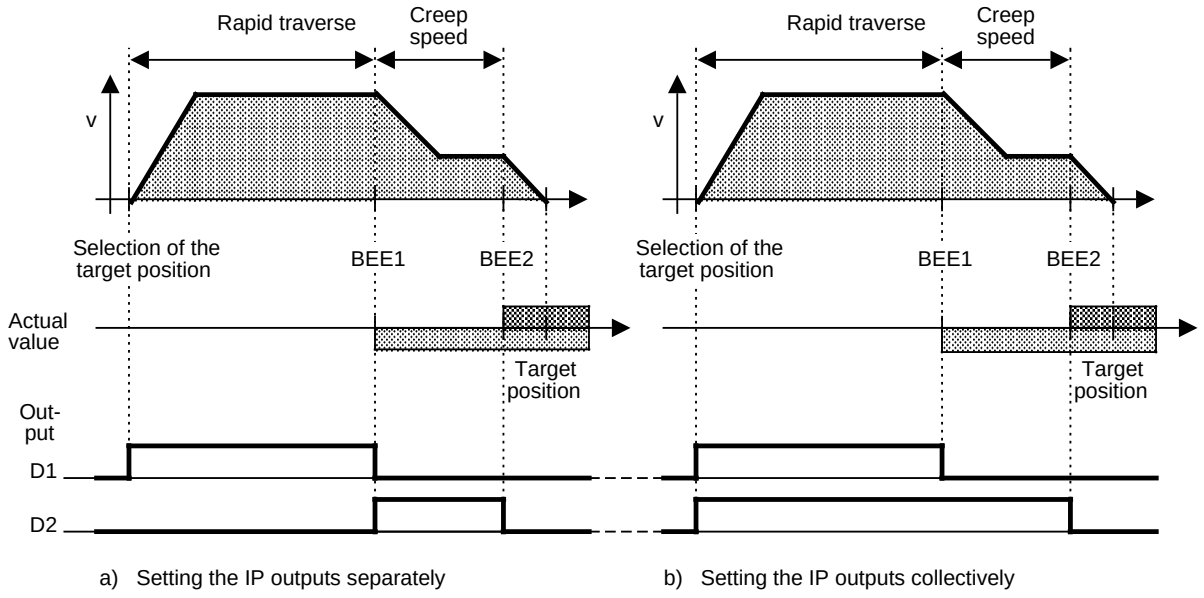
For a rotary axis, the IP 240 always chooses the direction so that the target position is reached along the shortest possible path. You can influence the range of the actual position by forwarding a zero offset to the IP.

Switching the IP outputs

The IP 240 is equipped with two digital outputs per channel. When a position has been selected, the IP 240 sets the enabled outputs autonomously and resets or disables them when the switching points are reached.

In order to better adapt the IP 240 to your application, you can specify how the outputs are to be switched when you configure the IP.

a) The IP outputs control the traverse speed
   The speed is switched from rapid traverse to creep speed when the BEE1 range is entered. The drive is switched off when the BEE2 range is entered.
   You can also specify whether the outputs are to be set separately (Fig. 10-6 a) or collectively (Fig. 10-6 b).



a) Setting the IP outputs separately b) Setting the IP outputs collectively

Fig. 10-6. IP Outputs Control the Traverse Speed

b) The IP outputs control the direction of travel
The IP 240 sets one or both outputs in dependence on the required direction of travel.
D1 is set if travel in positive direction is required.
D2 is set if travel in negative direction is required.
The drive is switched off when the BEE2 range is entered.

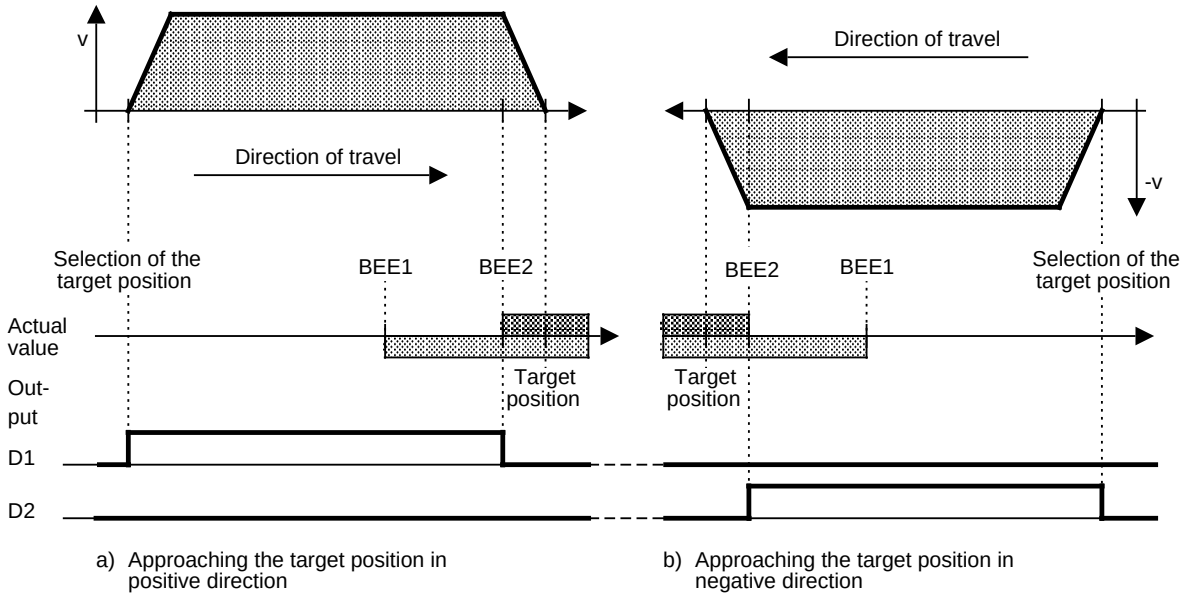


Fig. 10-7. IP Outputs Control the Direction of Travel

Two additional PLC digital outputs are required to control a drive with two speeds and two directions. These two outputs must be driven by the S5 CPU in dependence on status bit BEE1 for changing the speed or status bit RICH for controlling the direction.

Backlash compensation
Play in the drive system is referred to as backlash. Each time the direction is reversed, this backlash causes the motor to rotate without changing the position of the axis. If the position encoder is connected to the motor shaft, the result is a reduction in positioning accuracy.

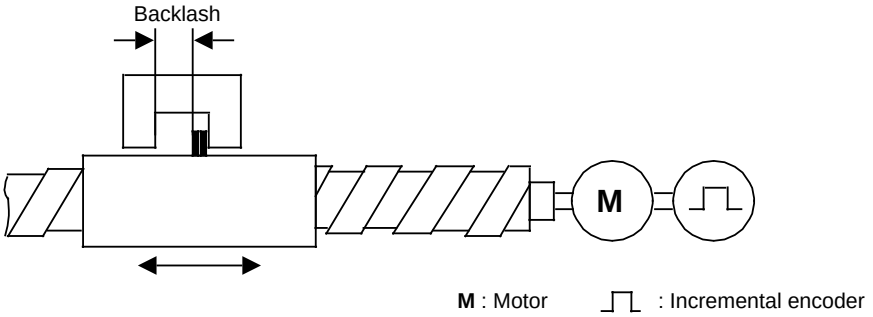


Fig. 10-8. Backlash

To compensate backlash, you can specify that the IP output is to be disabled on a approach to position only when the direction of travel was positive (ascending actual value). If the position was approached in a negative direction, the IP output remains set and the position is ”overrun”. When the BEE2 range is exited, the output must be reset over the S5 CPU (via embedded commands to the IP 240). The position must then be reselected.
With the same logic, synchronization is attained following an approach to reference point only when the reference point was reached from a positive direction.

Actual value-dependent interrupt generation
During configuring, you specify at which points on an approach to position the IP 250 is to generate interrupts. By reading the interrupt request bytes from the IP 240, you can react appropriately to the cause of the interrupt.
Interrupts can be generated at the following points:
- On entry into ranges BEE1, BEE2 and BEE3.
- Upon unintentional exiting of range BEE3 (target range exited).
- On exiting range BEE2 (reversal of direction to compensate for backlash possible).

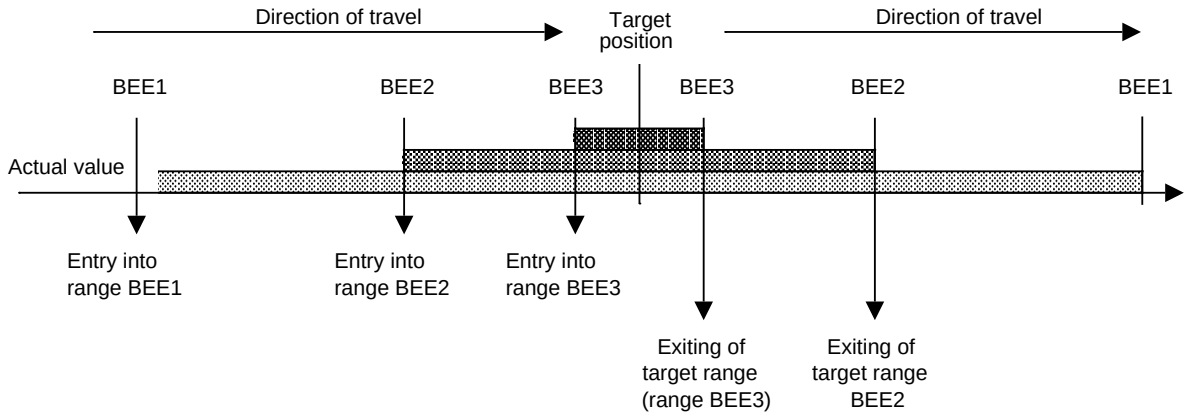


Fig. 10-9. Actual Value-Dependent Interrupt Generation

All interrupts are generated only once per selected position.

Methods of synchronization
Positioning with the IP 240 is possible only following synchronization of the actual value. Three methods of synchronization are available for this purpose.

a) Reference point approach
For reference point approach, you can calibrate the actual value to a fixed reference point in the traverse range with the aid of the incremental encoder's zero mark signal.
To make reference point approach possible, you must connect a preliminary contact switch to the IP 240's IN input.

b) Synchronization with an internal control bit
This method of synchronization is referred to in the following as software-controlled synchronization.
Each time a set control bit is transferred, you can reset the actual value and reactivate the position last selected. Positioning then begins immediately.

c) Synchronization with an external control signal
When this method is used, each positive signal edge at the IN input resets the actual value and reactivates the position last selected. Positioning can thus be started in dependence on the IN signal.
This method of synchronization is particularly suitable for length measurement, as the current actual value is stored as final value on a negative signal edge at the IN input.
Note that a complete module firmware cycle may intervene between the presence of the edges and processing of the edge change on the IP 240.

Any of these methods may be used. Each time synchronization takes place, the actual value is set to the value of the last zero offset that was transferred, thus redefining the reference point for the actual value.

10.2 Configuring the IP's Performance Characteristics

Sections 10.3 to 10.10 describe how to program the IP's performance characteristics, and also provide information on
- the data areas that are transferred to the IP 240 during configuring,
- how you must specify this data and
- how the data is evaluated on the IP 240.

To help you find the various configuring parameters easily and quickly, the relevant parameter is shown in parentheses in the section headers.

Standard function block FB 167 must be used to configure the IP 240 for ”positioning” mode. As this function block (FB) handles data interchange with the IP via a data block (DB), you must create this data block and enter the data to be transferred before invoking the FB.

You will find
- a summary of the contents of the data block in Section 10.23.1
- a summary of the parameters for FB 167 in Section 10.23.2

10.3 Numerical Representation

When you configure the IP 240, you can decide whether you want to work with binary or BCD numbers.

Binary representation
You can use binary numbers for all data required in positioning mode.
Signed binary numbers may assume positive or negative values. A negative value is represented as two's complement. The signal state of the most significant bit identifies the sign of the number. The sign bit is ”0” for a positive and ”1” for a negative number. All bit positions not needed to represent the number assume the value of the sign bit. These bits, and the sign bit, are referred to in the following as **sign extension** (SE).
Unsigned binary numbers are interpreted as absolute values, i.e. the most significant bit is also taken as part of the value.

BCD representation
If you require BCD-coded data for the purpose of documentation, definition or post-processing, you may choose this form of representation instead of binary. Position numbers and distance values for position 0, however, **cannot** be represented in BCD.
”1111” is entered in the high-order nibble (half-byte) as the sign (SG) of a negative number. A nibble (also called a half-byte or tetrad) is the term used for the four high-order or the four low-order bits in a byte.

> **Note**
>
> The IP 240 module firmware has to carry out format conversions to write and read BCD-coded data, which on-loads the firmware's cycle for a data interchange (Chapter 12, ”Response Times”).

The selected form of numerical representation must be taken into account for both data interchange using standard function blocks FB 167 and FB 168 and direct data interchange.

10.3.1 Specifying the Numerical Representation (BCD)

Configuring parameter BCD for FB 167 is used to specify the required form of numerical representation:

```
        :   JU FB 167
NAME    :   STRU.POS
        :
        :
BCD     :   KY  x,y        x or y=0    Numbers in binary
                           x or y=1    Numbers in BCD
```

In order to enable the numerical representation to be matched to the relevant requirements, a distinction was made between two data areas which are assigned as follows to parameters x and y:

x parameter	y parameter
Position values for positions 1 to 254	Position value for position 0
Distance values for positions 1 to 254	Zero offsets
Range limit value for the rotary axis	Actual value
	Final value, (= actual value stored when using ”Synchronization with external control signal” as synchronization method)

> **Note**
>
> The position numbers and the distance values for position 0 are always interpreted as unsigned binary numbers. BCD representation is not possible.

10.3.2 Data in the Data Block and in the Transfer Buffer

If the data interchange with the IP 240
- is handled by standard function blocks, you must observe the contents of the data words in the data block when writing and evaluating data.
- is programmed as direct data interchange (Chapter 11), you must observe the contents of the data bytes in the transfer buffer when writing and reading data.

The permissible value ranges of the various items of data determine the number of bytes needed to represent that item of data. Three ”lengths” are possible, irrespective of whether the data is forwarded in the data block or in the transfer buffer:
- four bytes
- two bytes
- one byte

The table below shows the general layout of the data in the data block and in the transfer buffer.
When data is entered in the data block, entry begins with the nth data word. DL n identifies the lefthand byte and DR n the righthand byte in data word ”n”.
The contents of the transfer buffer relate to the offset with which the byte is addressed. You can obtain the complete address by adding the offset to the module start address (Chapter 11, ”Direct Data Interchange”).

- 4-byte data
  Four bytes are provided for the following items of data:
  - Position values for positions 1 to 254
  - Distance values of ranges BEE1 to 3 for positions 1 to 254
  - Position value for position 0
  - Distance values of ranges BEE1 to 2 for position 0
  - Range limit value for the rotary axis
  - Zero offset
  - Actual value
  - Final value

Table 10-4. Layout of 4-Byte Data Items in the DB and in the Transfer Buffer

Data block	Byte layout	Offset in transfer buffer
DL n	Byte 1	0
DR n	Byte 2	1
DL n+1	Byte 3	2
DR n+1	Byte 4	3

Table 10-5. Numerical Representation of 4-Byte Data Items

Numerical representation		Byte 1		Byte 2		Byte 3		Byte 4	
Binary		SE		2^{23} to 2^{16}		2^{15} to 2^{8}		2^{7} to 2^{0}	
BCD	without sign	0	10^6	10^5	10^4	10^3	10^2	10^1	10^0
	with sign	SG	10^6	10^5	10^4	10^3	10^2	10^1	10^0

- 2-byte-data
  Two bytes are available for the following data items:
  - Distance value of range BEE3 for position 0

Table 10-6. Layout of a 2-Byte Data Item in the DB and in the Transfer Buffer

Data block	Byte layout	Offset in transfer buffer
DL n	Byte 1	0
DR n	Byte 2	1

Table 10-7. Numerical Representation of a 2-Byte Data Item

Numerical representation	Byte 1	Byte 2
Binary	2^{15} to 2^{8}	2^{7} to 2^{0}

- 1-byte-data
  One byte is available for the following data items:
  - Position number for selecting the next position (forwarded to IP)
  - Number of the active position (read out from IP)

Table 10-8. Layout of a 1-Byte Data Item in the DB and in the Transfer Buffer

Data block	Byte layout	Offset in transfer buffer
DL n	0	0
DR n	Byte 1	1

Table 10-9. Numerical Representation of a 1-Byte Data Item

Numerical representation	Byte 1
Binary	2^{7} to 2^{0}

Numerical representation and ranges for input and output values
The table below provides an overview of the digit positions actually used and of the ranges for all input and output values.
The table also shows, once again, in which cases you need binary and in which cases BCD representation for numerical values. In the column headed ”Configuring parameter” you will find the allocation of the data item to configuring parameter BCD/x or BCD/y.

Table 10-10. Numerical Representation of Input and Output Values

Numerical value	Binary	BCD	Permissible value range	Configuring parameter
Position values for positions 1 to 254	32 bits	7 decades and sign	-9,999,999 to +9,999,999	BCD/x
Distance values for positions 1 to 254	20 bits	6 decades	0 to 999,999	BCD/x
Range limit value for a rotary axis	24 bits	7 decades	1 to 9,999,999	BCD/x
Actual value	32 bits	7 decades and sign	-9,999,999 to +9,999,999	BCD/y
Final value	32 bits	7 decades and sign	-9,999,999 to +9,999,999	BCD/y
Zero offset	32 bits	7 decades and sign	-9,999,999 to +9,999,999	BCD/y
Position value for position 0	32 bits	7 decades and sign	-9,999,999 to +9,999,999	BCD/y
Distance value BEE1 and BEE2 for position 0	20 bits	(not possible)	0 to 999,999	-
Distance value BEE3 for position 0	16 bits	(not possible)	0 to 65,535	-
Position numbers	8 bits	(not possible)	0 to 255	-

10.4 Axis Types

The IP 240 can be used in conjunction with a linear or a rotary axis.

10.4.1 Linear Axis

When a linear axis is used, the traverse path is delimited by two end points. The maximum traversing range results from the permissible actual value range of - 9,999,999 to +9,999,999 increments.

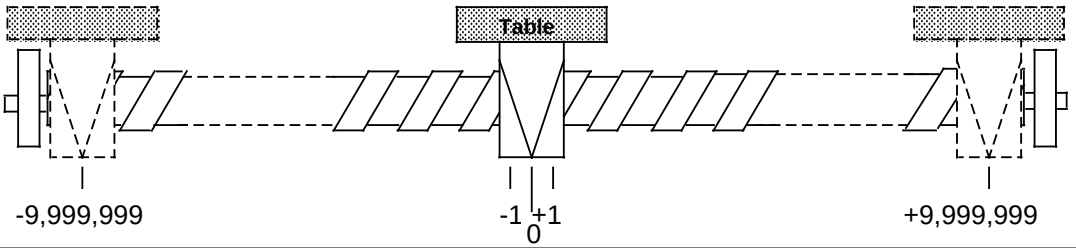


Figure 10-10. Linear Axis

10.4.2 Rotary Axis

In the case of a rotary axis, the traverse path is closed and is not limited. A revolution can comprise a maximum of 9,999,999 increments.

The rotary axis is defined by the following values:
- The **initial value** of the rotary axis is always ”0”.
- The **final value** of the rotary axis points to the same position as the initial value. It must be assigned in the configuration of the IP 240 and may lie between +1 and +9,999,999.
- The **maximum counting value** marks the highest displayable value. It is the result of:

maximum counting value of the rotary axis = final value -1

All positioning values must lie between ”0” and [final value - 1]

Positioning with ascending actual value (positive direction)
If the actual value reaches the maximum counting value for the rotary axis, the count is continued with actual value ”0”.
Positioning with descending actual value (negative direction):
If the actual value reaches ”0”, counting is continued with the maximum counting value for the rotary axis.

Example: Assuming a final value of 3600, the counting sequence is as follows:

- positive direction:	...	3597	3598	3599	0	1	2	3	...
- negative direction:	...	3	2	1	0	3599	3598	3597	...

Half of the final value is permitted as maximum distance for ranges BEE1 to BEE3, but may not exceed 999,999 increments (distance for range BEE1 0.5·[final value for the rotary axis]).

To offset the zero point, you can specify a positive or negative zero offset (NVER). However, the zero offset value may not exceed the final value specified for the rotary axis (NVER +/- [final value for the rotary axis]).

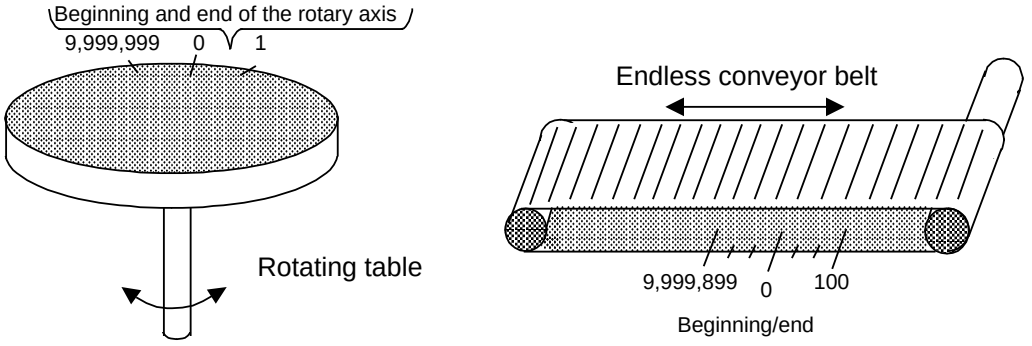


Fig. 10-11. Rotary Axis

Warning

When a position has been selected, the IP 240 always chooses the direction of travel so as to reach the new setpoint over the shortest possible path. It bases its choices on the assumption that the component to be positioned can be rotated without restriction in both directions. If there is a restriction (such as the length of a cable), the IP 240 must be configured for a linear axis.

Maximum traversing speed
The encoder pulses acquired by the IP are counted in a counter chip. The current (internal) count is read once in every module firmware cycle and is then post-processed to form the (external) actual value.
In order for the IP 240 module firmware to ascertain the direction of movement without any ambiguity whatsoever, the change in the actual value between two count readouts (t_{LZ}) must be less than the halved final value for the rotary axis ($t_{LZ\ max.} \cdot v_{\ max.} < 0.5 \cdot$ [final value for the rotary axis]).
The max. amount of time between two count readouts from the counter chip is computed as follows:

$t_{LZ\ max.} = t_{ka1\ max.} + t_{ka2\ max.} + 2 \cdot t_{kom\ max.}$

$t_{ka1\ max.}$ = Maximum processing time for channel 1
$t_{ka2\ max.}$ = Maximum processing time for channel 2
$t_{kom\ max.}$ = Maximum amount of time needed for a data interchange

In Chapter 12, "Response Times", you will find a list of processing/execution times to help you compute the permissible traversing speed for your application. When the maximum amount of time is assumed for processing channel 1 and channel 2 and for the data interchange, $t_{LZ\ max.}$ computes to 7.5 ms.
When computing the traversing speed, also refer to the information presented in Section 10.8.2 "Distance values for the switching and signalling ranges".

10.4.3 Specifying the Axis Type and the Final Value for the Rotary Axis (RUND)

The axis type is specified during configuring using the RUND parameter:

	:	JU FB 167		
NAME	:	STRU.POS		
	:			
	:			
RUND	:	KF x	x=0	The channel is configured for a linear axis
			x=1	The channel is configured for a rotary axis

If the channel is configured for a rotary axis, the final value for the axis must be entered in data words DW 48 and DW 49 of the data block. Configuring FB 167 transfers this value to the IP, and it cannot be changed following configuring.

Permissible range of the final value for the rotary axis: 1 to 9,999,999

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 48	0	0	0	0	0	0	0	0	0				10^6			
DR 48	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
DL 49	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DR 49	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			

10.5 Switching the IP Outputs

The IP 240 is equipped with two digital outputs (D1 and D2) for each channel.
You have two options for influencing setting and resetting of the IP outputs:

- You can determine the switching performance of the IP outputs when you configure the channel. Depending on the application, you can control either the direction of travel or the traversing speed directly via the IP outputs.
- After configuring, you can define the state of the outputs via the S5 CPU using embedded commands, or you can can let the IP 240 control the outputs on an actual value-dependent basis (Section 10.15.1 ”Controlling the IP Outputs”).

The following applies for the flow diagrams in this section:

- The outputs are controlled by the IP 240 dependent on the actual value
- The IP 240 enables the outputs so that they can be set.

10.5.1 Selecting the Switching Performance of the IP Outputs (DAV)

You have three configuring options for matching the IP 240 to your application:

	:	JU FB 167		
NAME	:	STRU.POS		
	:			
	:			
DAV	:	KF x	x=0	IP outputs control the traversing speed, outputs are switched separately Output D1 controls rapid traverse Output D2 controls creep speed
			x=1	IP outputs control the traversing speed, outputs are switched collectively Output D1 and output D2 control rapid traverse Output D2 controls creep speed
			x=2	IP outputs control the direction Output D1 controls positive direction Output D2 controls negative direction

Note

The IP 240 takes the configured switching performance into account during positioning and reference point approach.

10.5.2 The IP Outputs Control the Traversing Speed

When you configure DAV=0 or DAV=1, you pass control of the traversing speed to the IP outputs. The outputs are switched without regard to the direction of travel.

a) **Outputs are set separately (DAV=0)**
After the target position has been selected (Fig. 10-12a: Actual value 1000), the IP 240 sets output D1 in dependence on the actual value. When range BEE1 is entered (actual value 2000), output D1 is reset and output D2 set. When range BEE2 is reached (actual value 3000), output D2 is reset.

b) **Outputs are set collectively (DAV=1)**
When the target position has been selected (Fig. 10-12b: Actual value 1000), the IP 240 sets inputs D1 and D2 in dependence on the actual value. Output D1 is reset when range BEE1 (actual value 2000) is entered, output D2 when range BEE2 (actual value 3000) is entered.

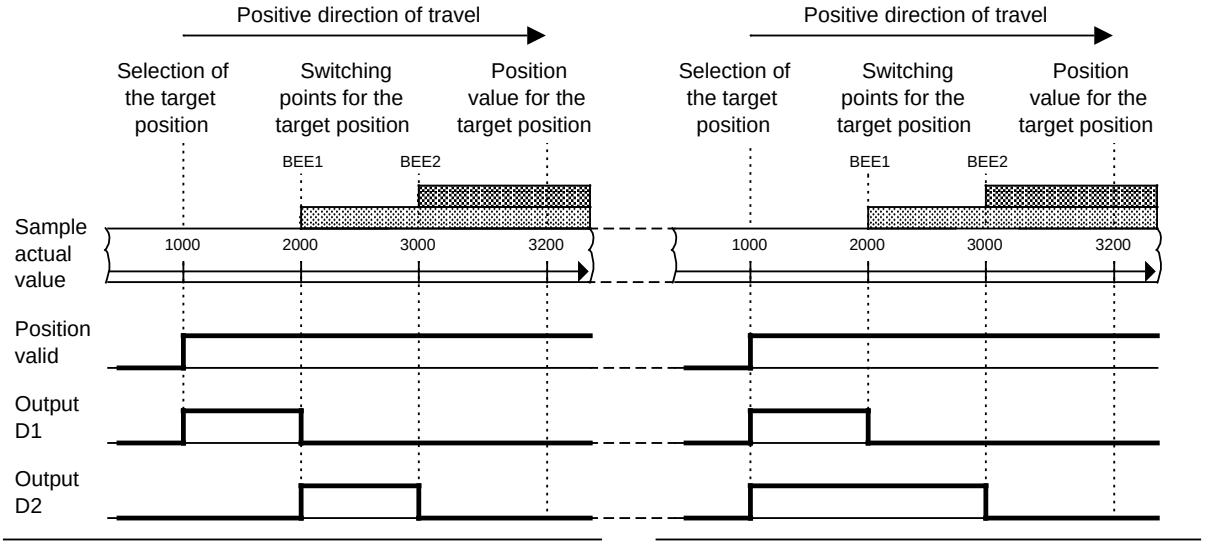


Fig. 10-12a. Switching Performance of the IP Outputs when DAV=0

Fig. 10-12b. Switching Performance of the IP Outputs when DAV=1

To define the direction of travel, you can scan status bit RICH (direction) on the IP 240 on a one-shot basis after selecting the position and use it to control two additional PLC digital outputs via the S5 CPU.

10.5.3 The IP Outputs Control the Direction of Travel

When you choose this option, the IP outputs are allocated to the direction of travel.
When the target position is selected, the IP 240 computes the direction of travel from the actual value and the position value for the target position and sets one of the IP outputs.
Output D1 is set if positive travel (ascending actual value) is required (Fig. 10-13a: Actual value 1000).
Output D2 is set if negative travel (descending actual value) is required (Fig. 10-13b: Actual value 6000).
The output that was set is reset when range BEE2 is entered (Fig. 10-13a: Actual value 3000, Fig. 10-13b: Actual value 4000).

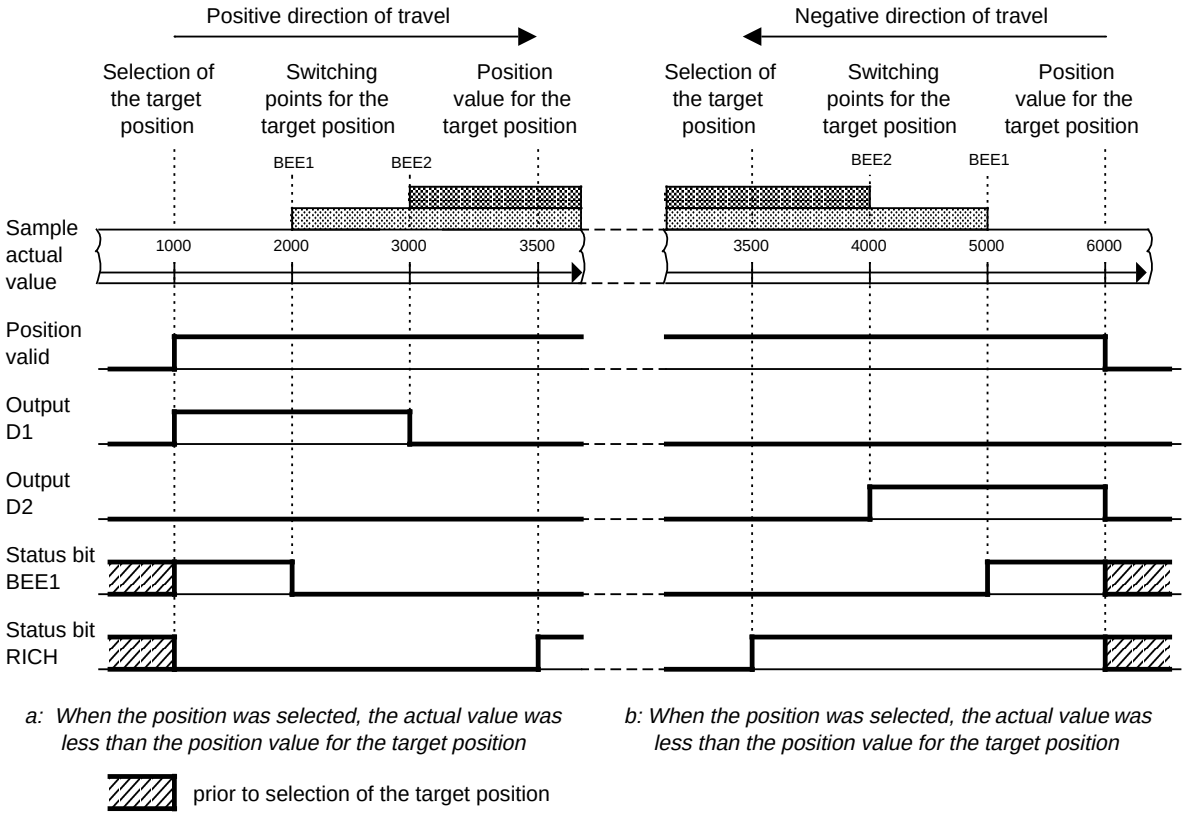


Fig. 10-13. Switching Performance of the IP Outputs when DAV=2

To monitor switching of the traversing speed, you can scan status bit BEE1 cyclically on the IP 240 after positioning has started or evaluate the interrupt (BE1) generated by the negative edge of the BEE1 bit. In this way, you can control two additional PLC digital outputs over the S5 CPU.

Note

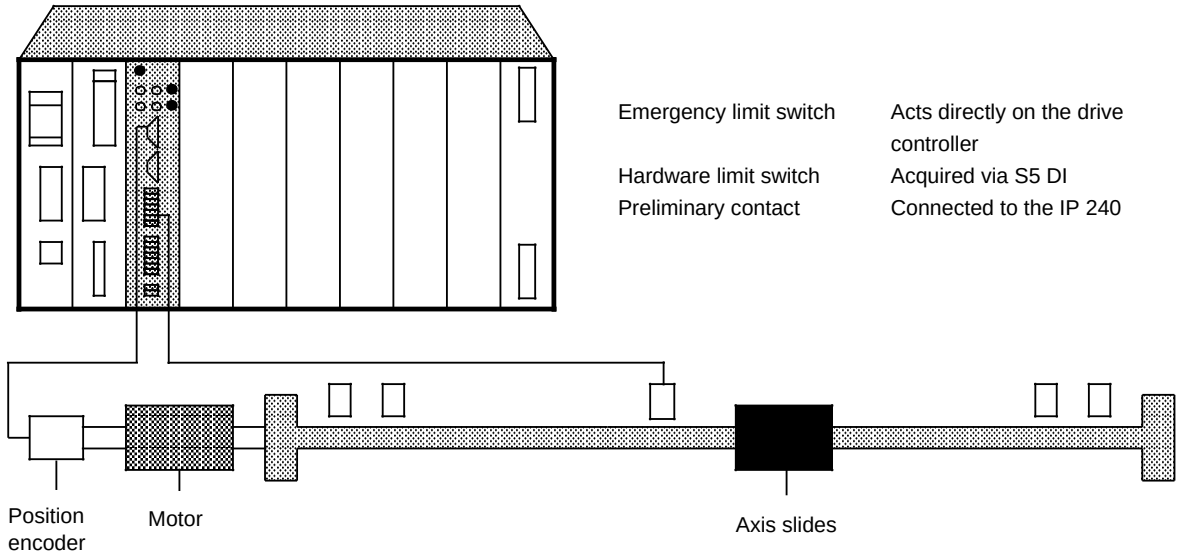
In the case of a rotary axis, the IP 240 always switches the outputs so that the target position is reached over the shortest possible path.

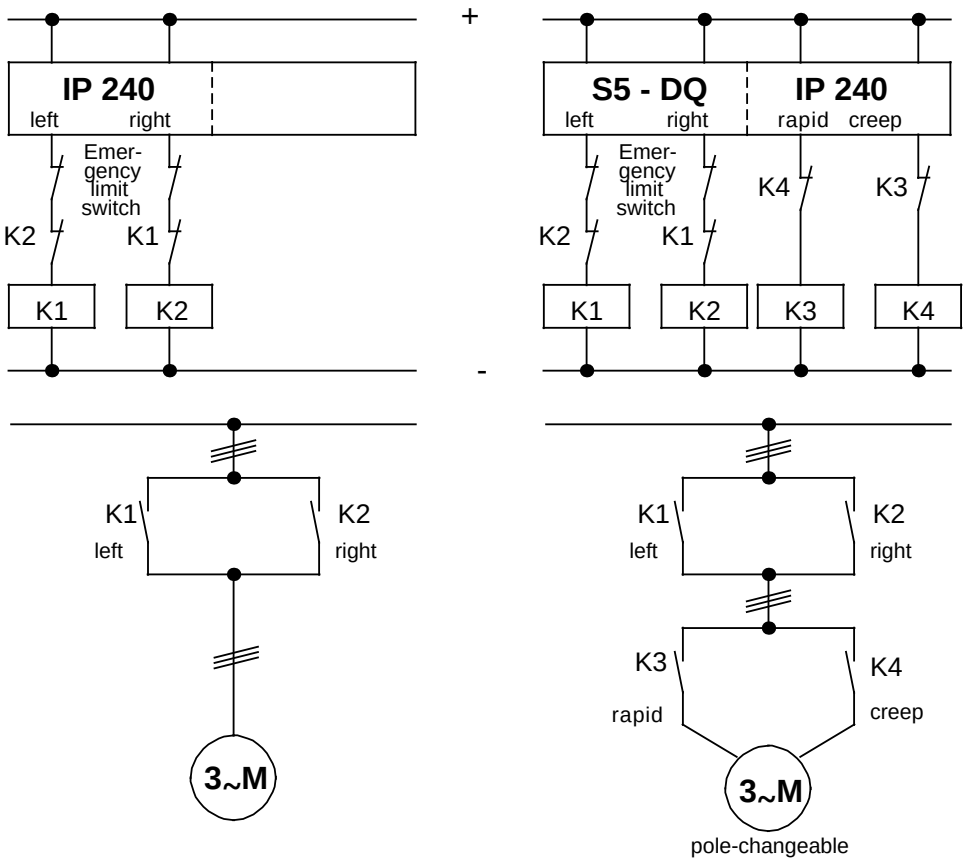
10.5.4 Recommendations for Selecting the Switching Performance

It is recommended that the IP outputs show the following switching performance when the IP is used for axis control:

Table 10-11. Recommendations for Selecting the Switching Performance of the IP Outputs

	One direction of travel	Two directions of travel
One traversing speed	The IP outputs control the traversing speed	The IP outputs control the direction of travel
Two traversing speeds	The IP outputs control the traversing speed	The IP outputs control the traversing speed





a) IP 240 controls direction of travel b) IP 240 controls traversing speed

Fig. 10-14. Contactor Control of a Three-Phase Motor

10.6 Backlash Compensation (LOSE)

Backlash in the position decoding system reduces the positioning accuracy. To prevent this, all positions and the reference point must always be approached from the same direction. The IP 240 supports this when you configure ”Backlash compensation”.

Configuring backlash compensation
You can specify backlash compensation by setting the ”LOSE” parameter to ”1”:

	:	JU FB 167		
NAME	:	STRU.POS		
	:			
	:			
LOSE	:	KF x	x=0	No backlash compensation; the direction of movement is not to be evaluated when range BEE2 is entered.
			x=1	Backlash compensation; the direction of movement is to be evaluated when range BEE2 is entered.

10.6.1 Backlash Compensation during Positioning

When you configure ”LOSE”=1, you stipulate that positions may be approached in a positive direction only (ascending actual value).
To determine the direction of travel, the change in the actual value on entering range BEE2 is computed on the IP 240 over a module firmware cycle. If the IP identifies a positive direction of travel, positioning proceeds normally.
If the IP identifies a negative direction of travel,

- the IP output is not reset.
- interrupts BE2 (range BEE2 entered) and BE3 (range BEE3 entered) are not generated.
- status bit ZBEV is not set and the associated interrupt ZBV is not generated when the target range (range BEE3) is exited.

When range BEE2 is exited, the IP 240 indicates that the position can be reselected by setting status bit RIUM and generating interrupt RIU.

If the direction of travel changes to negative after range BEE2 has been entered, the status and interrupt bits are not affected (ZBEV is not set; interrupts BE2, BE3 and ZBV are not generated).

> **Note**
>
> Backlash compensation does not affect the setting and resetting of status bits BEE1, BEE2 and BEE3.
> When the position has been ”overrun”, the IP 240 signals that range BEE2 has been exited. The IP output that is still active can be disabled via the STEP 5 program by setting the FREI control bit to ”0” and forwarding it to the IP 240 (Section 10.15.1 ”Controlling the IP Outputs”).

If the actual value is greater than the position value of a newly selected position, the positioning procedure must be subdivided into two steps:

1st step

Select position (Fig. 10-15: Actual value 9300).

The drive is switched on and moves at rapid traverse speed in a negative direction toward the target position.

The speed is switched to creep at the right BEE1 switching point (actual value 7400).

The drive is **not** switched off at the right BEE2 switching point (actual value 5300), as the BEE2 range was approached in a negative direction.

When the position has been ”overrun”, the IP 240 signals that the reversal point has been reached (BEE2 exited, actual value 4700) by setting status bit RIUM and the associated interrupt bit RIU.

Control bit FREI=0 must now be transferred via the STEP 5 program to disable the IP output (actual value 3400 or 1900).

2nd step

Select the same position once again.

The drive approaches the position in a positive direction. When the switching and signalling ranges are entered, the configured interrupts are generated.

The module firmware disables the IP output at switching point BEE2 (actual value 4700).

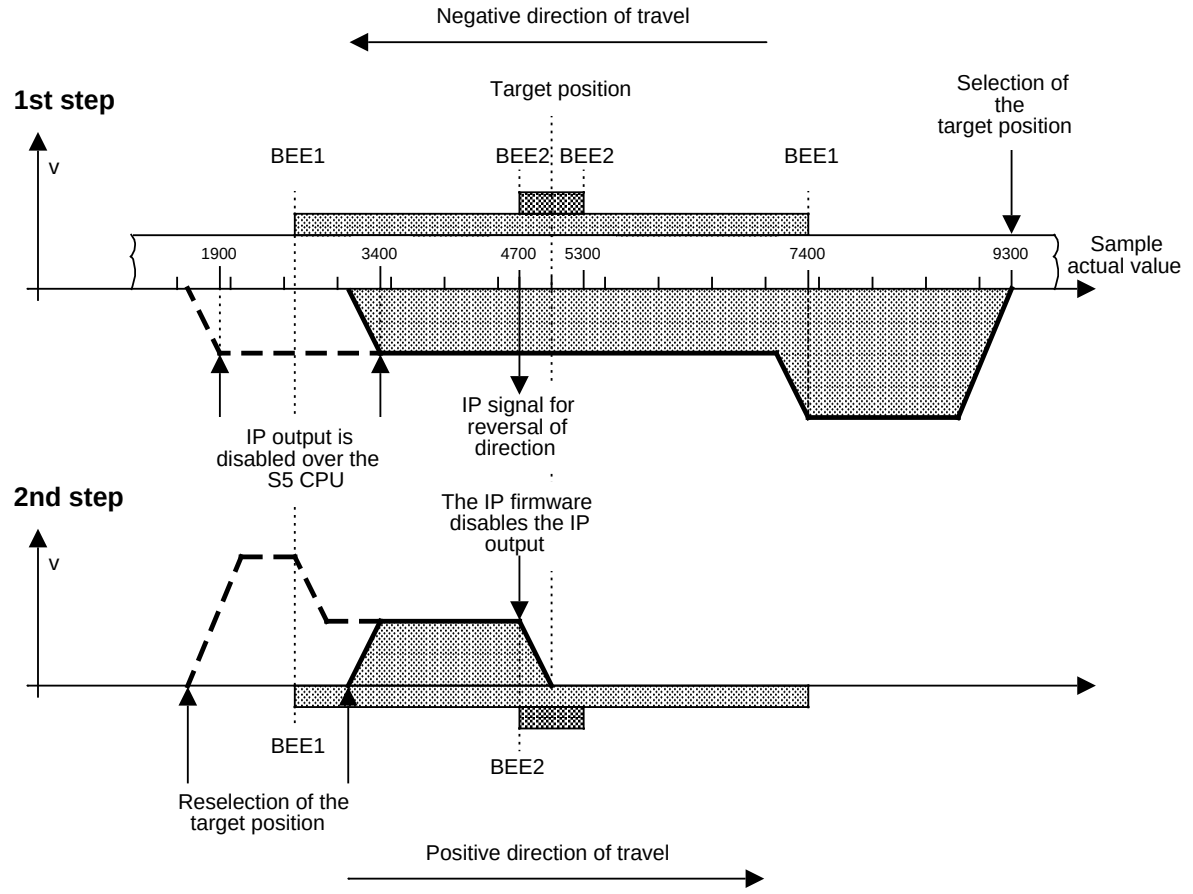


Fig. 10-15. Approaching a Position with Backlash Compensation

10.6.2 Backlash Compensation during Reference Point Approach

Compensation of the backlash during reference point approach (Section 10.13.1) is similar to compensation during positioning.
Synchronization is attained only when the reference point is approached in a positive direction. Decisive for evaluation of the direction is the instant at which the preliminary contact signal (connected to the IP's IN input) changes back to zero.

Since the position is normally not known following power-up, the approach to the reference point is normally begun after traversing to a starting point. The actual value of the starting point must therefore be less than the negative edge of the preliminary contact signal.
The direction of travel for reference point approach must always be specified by the S5 CPU.

> **Note**
>
> In order to ensure that synchronization is always done at the same place, the direction of travel for the reference point approach may not be changed following the negative edge at the IN input until the zero mark has been reached (synchronization).

10.7 Actual Value Generation

The IP 240 computes an internal signed count by counting the encoder pulses and evaluating the phase displacement between encoder pulse trains A and B. You can influence the conversion of this count into the actual value by
- configuring the required resolution and
- specifying a zero offset.

The actual value stored on the IP 240 is updated in every module firmware cycle, and can be read out over the S5 CPU.

Counting direction
The IP 240 counts the acquired encoder pulses
- up when the **B signal** is the leading signal.
- down when the **A signal** is the leading signal.

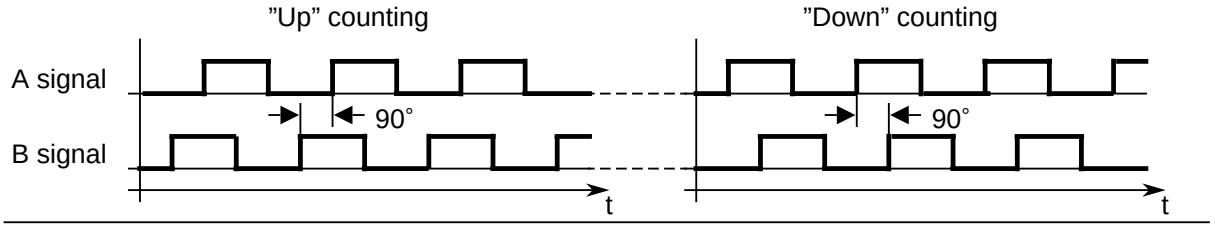


Fig. 10-16. Counting Direction in Positioning Mode

Changing the counting direction
To change the counting direction, you must interchange the following:
- for symmetrical encoders, interchange A/A $\overline{a}$nd B/$\overline{B}$
- for asymmetrical encoders, interchange A* and B*

Actual value range and overrange
The actual value range is defined as -9,999, 999 to +9,999,999.

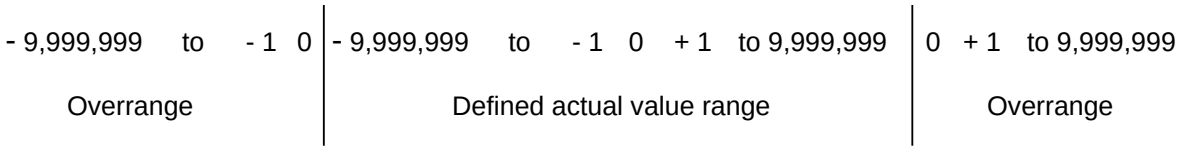


Fig. 10-17. Actual Value Range and Overrange in Positioning Mode

When the defined actual value range is exited, the counter enters the overrange and the IP 240 sets the **UEBL** bit. In the overrange, pulse acquisition (counting) proceeds as in the defined actual value range.
Since synchronization of the actual value is lost when the counter enters the overrange,
- synchonization bit SYNC is reset,
- comparison of the actual value with the switching and signalling ranges is stopped,
- the outputs are disabled,
- range bits BEE1 to 3 and direction bit RICH are set to ”1”
- and the selected position is declared invalid.

Status bit UEBL can trigger an interrupt if you initialized the PRA2 parameter accordingly when you configured the channel (Section 10.10). The associated interrupt bit (UEB) is reset in the interrupt request bytes.
Status bit UEBL is reset on the IP when the status area was read once with UEBL=1 or when the interrupt request bytes were read and it was the overrange that triggered the interrupt.

10.7.1 Resolution (AFL)

During configuring, you can specify an increment multiplication to match the resolution (travel per increment) to the traversing range. Accuracy can be increased by a twofold or fourfold increase in the resolution. The available traversing range (maximum path) is thereby reduced by a factor of 2 or 4. Each increment decrements or increments the actual value by one.

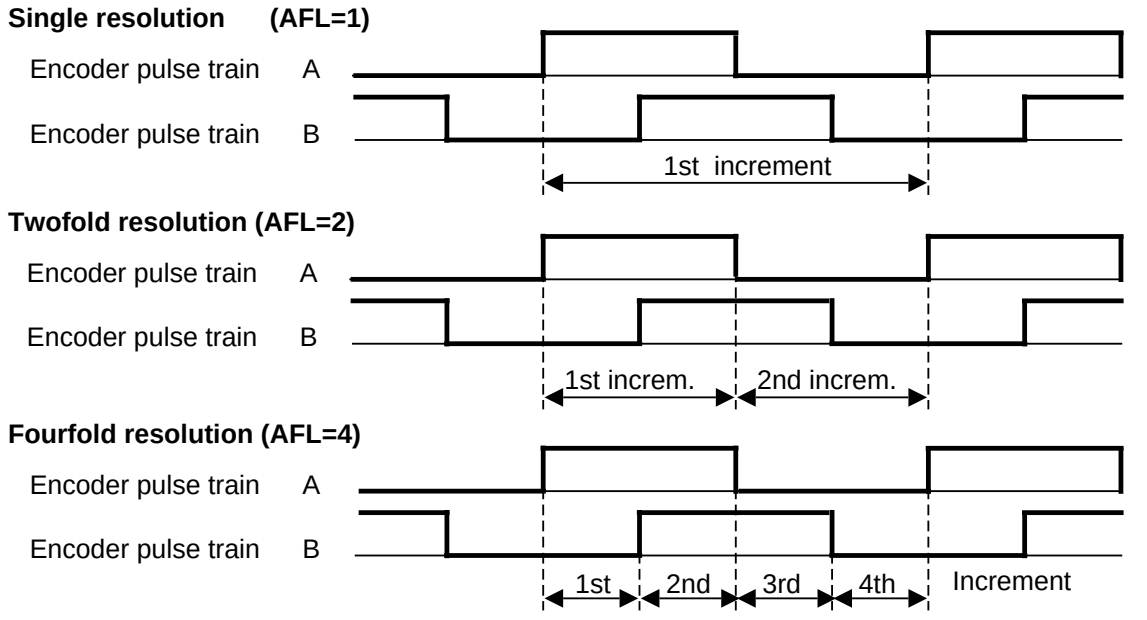


Fig. 10-18. Evaluation of the Encoder Pulses

You specify the resolution in configuring parameter **AFL**:

```
        :  JU FB 167
NAME    :  STRU.POS
        :
        :
AFL     :  KF x      x=1   Single resolution
                     x=2   Twofold resolution
                     x=4   Fourfold resolution
```

Example for a linear axis:
An incremental encoder supplies 2500 pulses/revolution. The leadscrew has a pitch of 5 mm/revolution. The position encoder thus supplies 2500 pulses for a path of 5 mm. The IP 240 can process up to 19,999,998 increments within the permissible actual value range (-9,999,999 to+9,999,999).
An AFL value of ”4” thus computes to the following values for the maximum traversing range and the travel per increment.

$$\text{Traversing range} = \frac{\text{Max. number of increments}}{\text{Specified resolution}} \cdot \frac{\text{Travel/encoder revolution}}{\text{Pulses/encoder revolution}}$$

⇓

where:

Max. number of increments	=	19,999,998 (increments)
Specified resolution	=	4 (increments/pulse)
Travel/encoder revolution	=	5 mm
Pulses/encoder revolution	=	2500 (pulses)

Max. traversing range=9,999,999 mm

$$\text{Travel per increment} = \frac{\text{Travel/encoder revolution}}{\text{Pulses/encoder revolution} \cdot \text{Specified resolution}}$$

⇓ using the values above

Travel per increment=0.5 µm

Table 10-12. Example: Traversing Ranges for an Encoder with 2500 Pulses/Revolution

Resolution	Traversing ranges	Travel/increment
Single	39,999,9 mm	2.0 µm
Twofold	19,999,9 mm	1.0 µm
Fourfold	9,999,9 mm	0.5 µm

10.7.2 Zero Offset

By transferring a zero offset (NVER), you can allocate a new actual value to the current position. You may also make a distinction as to whether or not actual-value matching should take the last (old) zero offset that was transferred into account.
The specified zero offset is taken into account when the actual value is computed and during synchronization of the actual value.

a) **Relative zero offset**
The new actual value is computed as followed when you specify a relative zero offset:

$$Actual_{\mathbf{new}} = Actual_{\mathbf{old}} + Zero\ offset_{\mathbf{rel.,new}} - Zero\ offset_{\mathbf{rel.,old}}$$

The actual value thus changes by the difference between the old and the new zero offset, thus ensuring that the zero offset last transferred always mirrors the distance value between the zero point of the actual value range and the reference point. If a zero offset of 0 is specified, the position at which the actual value=0 is the reference point.

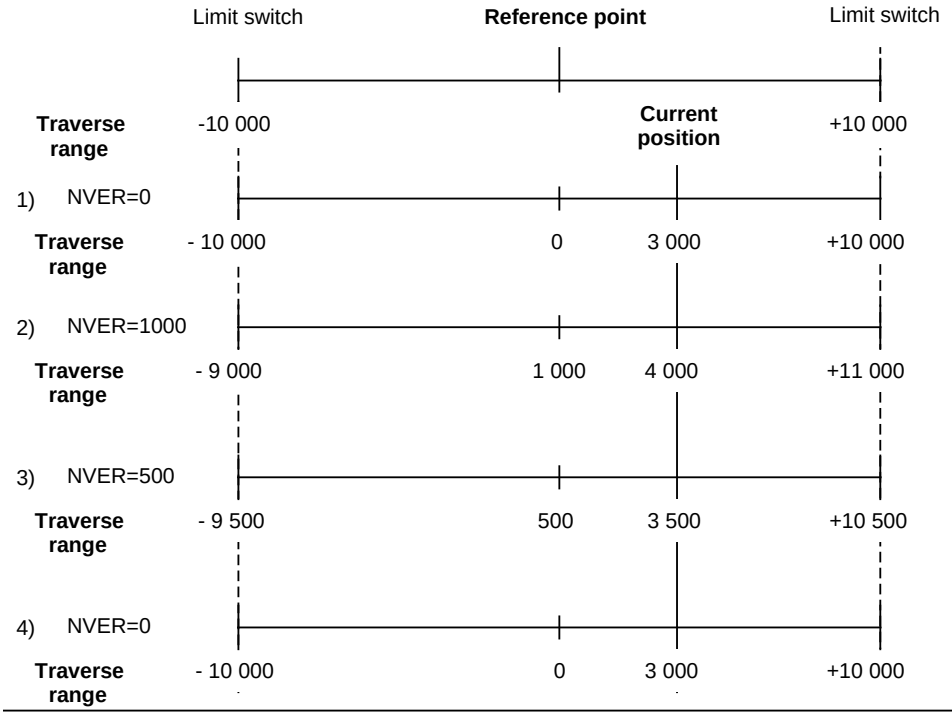


Fig. 10-19. Relative Zero Offset

Explanation: The values NVER=0, NVER=1000, NVER=500 and NVER=0 were transferred in succession as relative zero offset.

Note

When defining a zero offset, care must be taken that the entire traversing range is covered by the actual value and that the actual value does not enter the overrange.

b) **Additive zero offset**
The new actual value is computed as follows when you specify an **additive** zero offset:

$$Actual_{new} = Actual_{old} + Zero\ offset_{add.,new}$$

The actual value thus changes by the value of the additive zero offset transferred.

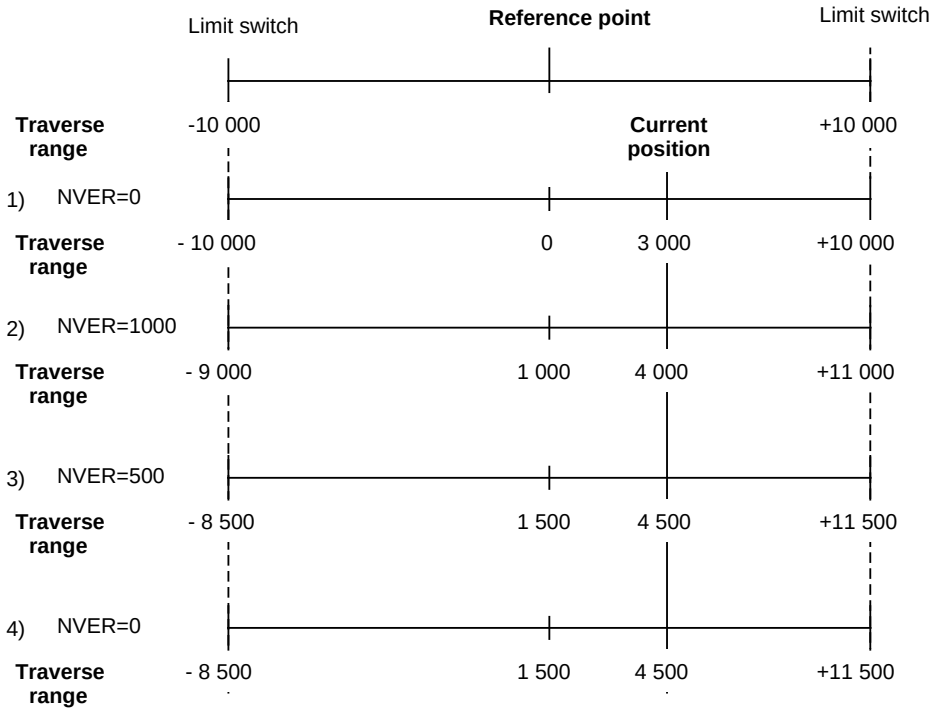


Fig. 10-20. Additive Zero Offset

Explanation: The values NVER=0, NVER=1000, NVER=500 and NVER=0 were transferred in succession as additive zero offset.

Specifying the zero offset
When you structure the channel, the zero offset (NVER) is transferred to the IP 240 in data words 46 to 47. You can change the zero offset after configuring.

Note the following when specifying the zero offset:
- If the channel is configured for a linear axis, NVER may be in the range from - 9,999,999 to + 9,999,999
- If the channel is configured for a rotary axis, NVER must lie between +/- [final value for the rotary axis].

In addition to the value for NVER, you must also specify the type of zero offset in D45/0 of the data block (ADD bit).
ADD=0 for a relative zero offset
ADD=1 for an additive zero offset

The table below shows the contents of the data block for a zero offset.

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DR 45	0	0	0	0	0	0	0	ADD	0	0	0	0	0	0	0	ADD
DL 46	SE	SE	SE	SE	SE	SE	SE	SE	SG				10^6			
DR 46	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
DL 47	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DR 47	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			
	A negative value must be specified as two's complement. SE=Sign extension								The high-order nibble of DL 46 (SG) must be ”1111” for a negative number.							

ADD=0 for relative NVER, ADD=1 for additive NVER

After configuring and after every synchronization, the actual value is set to the value of the last zero offset transferred, irrespective of whether the zero offset was relative or additive.
If you configured a channel for a rotary axis and transferred a negative zero offset, the actual value is set to the value [final value for the rotary axis] + [negative zero offset].

Example:

Final value of the rotary axis	=	10,000
Zero offset	=	- 2,000
Actual value after synchronization	=	8,000

Note

After configuring, you can transfer relative or additive zero offsets in any order. Note, however, that, after an additive zero offset, the next relative zero offset sets NVER $_{\mathbf{rel.,old}}$ to 0 (Section 10.18.3).

10.8 Position Data for Positions 1 to 254

Position data includes:
- the position value designating the absolute location of the position in the traversing range,
- the position number, which you use to select a position,
- the distance values of the switching and signalling ranges.

Position data for a total of 254 positions can be stored on the IP for each channel. The distance values for the switching and signalling ranges apply to all positions.

> **Note**
>
> Position 0 is also available as additional position. Position 0 is not stored on the IP. In contrast to positions 1 to 254, position 0 can be selected when the IP outputs for the channel are set (Section 10.14.2).

10.8.1 Position Value and Position Number

The position value defines the absolute location of the position in the traversing range. This value refers to the zero point of the actual value range (actual value=0).
Permissible values for a position value:
- between - 9,999,999 and+9,999,999 for a linear axis
- between 0 and +[final value of the rotary axis - 1] for a rotary axis

Each position value is assigned a position number which you define during configuring. You can select a position over the position number.
Permissible values for a position number: 1 to 254

So that there are no ambiguities in the allocation of position value to position number, each position number may be defined only once. An error message is issued should you fail to observe this rule.

Transferring position values and position numbers with the configuring FB
The position data is initially transferred to the IP 240 when you configure the channel. After configuring, you can change the position values again. The inclusion of new position numbers or the modification of old position numbers is not possible. Before invoking FB 167, you must enter the position values, the position numbers and the number of positions to be transferred in the data block.

The number of positions to be transferred must be entered in DW 58.

Binary representation

Data byte	Bit 7	6	5	4	3	2	1	0
DL 58 DR 58	0 2^7	0 2^6	0 2^5	0 2^4	0 2^3	0 2^2	0 2^1	0 2^0

Permissible range of values: 0 to 254

Entering the position numbers and position values in the data block

The area beginning with DW 60 is reserved for position numbers and position values. The number of positions determines the length of the data block (Section 10.23.1). If you need more than 65 positions, then you also need more than 256 data words in the DB. Observe carefully the restrictions applying to processing of data words beyond DW 255 (Section 10.24).

A position entry (position number and position value) always reserves three contiguous data words in the data block. In the tables below, the variable n identifies the first word for a position entry.

The first position entry begins at data word 60.

1st	position entry	:	DW 60	to	DW 62	(n=60)
	DW 60	:	Position number			
	DW 61 to 62	:	Position value			
2nd	position entry	:	DW 63	to	DW 65	(n=63)
3rd	position entry	:	DW 66	to	DW 68	(n=66)
		:				
254th	position entry	:	DW 819	to	DW 821	(n=819)

Position numbers in the data block

Binary representation

Data byte	Bit 7	6	5	4	3	2	1	0
DL n	0	0	0	0	0	0	0	0
DR n	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Permissible value range: 1 to 254

Position values in the data block

Binary representation / BCD representation

Data byte	Bit 7	6	5	4	3	2	1	0	Bit 7	6	5	4	3	2	1	0
DL n+1	SE	SE	SE	SE	SE	SE	SE	SE	SG				10^6			
DR n+1	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
DL n+2	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DR n+2	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			
	Negative values must be given as two's complement. SE=Sign extension								The high-order nibble of DL n+1 (SG) must be ”1111” for a negative number.							

Permissible value ranges:

- Between - 9,999,999 and +9,999,999 for a linear axis
- Between 0 and +[final value of rotary axis - 1] for a rotary axis

Note

When you attempt to define position number ”255”, the IP 240 does not evaluate transfer the position value.

The position number assigned to a position need not be identical to the number of the position entry.
It is more practical, however, for the two to be identical, particularly when you want to change a position value with control FB 168 after configuring (Section 10.18.1), as the number of the position entry, not the position number itself, must be specified in the control FB.

10.8.2 Distance Values of the Switching and Signalling Ranges

The distance values for the switching and signalling ranges for positions 1 to 254 are stored on the IP, and apply for all of these positions.
When a position number is selected, the IP 240 takes the position value of the new target position as setpoint and computes the locations of the switching and signalling ranges from the distance values. These ranges are symmetrical to the position value.

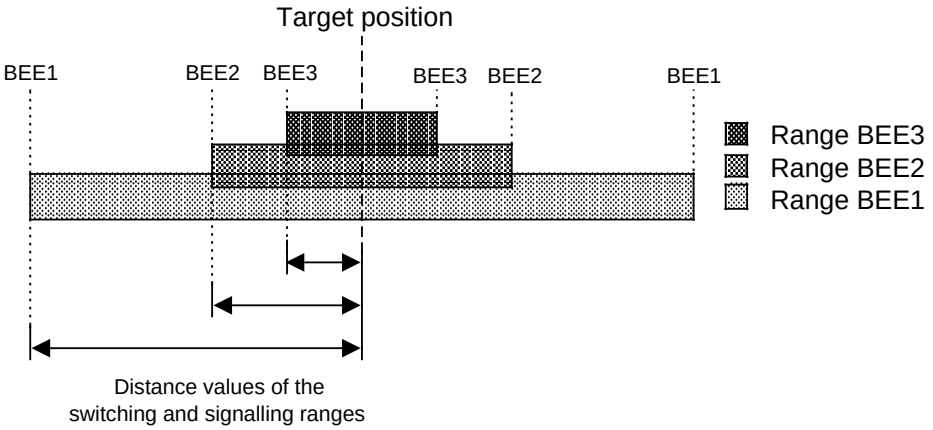


Fig. 10-21. Position Setup

Example:
The following distance values were defined for a position value of 10,000 increments:
Distance value to range BEE1 = 4,000 increments
Distance value to range BEE2 = 1,000 increments
Distance value to range BEE3 = 500 increments

These values compute to the following ranges:
Range BEE1 Low limit=6,000 and high limit=14,000
Range BEE2 Low limit=9,000 and high limit=11,000
Range BEE3 Low limit=9,500 and high limit=10,500

The lower and upper limits are part of the range.

When the actual value is within a range, the associated status bit BEE1, BEE2 or BEE3 is set to zero. Changes in the values of these bits can trigger the following responses from the IP during approach to a position:

Table 10-13. Switching of the IP Outputs and Triggering Interrupts during Approach to Position

Switching of the IP outputs	BEE1 from 1 0	BEE2 from 1 0	BEE3 from 1 0	BEE3 from 0 1	BEE2 from 0 1
DAV=0	DA1 is reset DA2 is set	DA2 is reset	___	___	___
DAV=1	DA1 is reset	DA2 is reset	___	___	___
DAV=2		DA1 or DA2 is reset	___	___	___
Interrupts	Range BEE1 entered (BE1)	Range BEE2 entered (BE2)	Range BEE3 entered (BE3)	Range BEE3 exited (ZBV)	Range BEE2 exited (RIU)

Signal from 0 1: Rising signal edge
Signal from 1 0: Falling signal edge

The following must be taken into account when defining the distance values:

- Distance value to BEE1 distance value to BEE2 distance value to BEE3
- Module firmware execution times.
  In each firmware cycle, the IP 240 compares the actual value with the limit values for the switching and signalling ranges. You must select a traversing speed and distance values that enable the IP 240 to recognize the various zones (e.g. between switching point BEE1 and switching point BEE2).

  The maximum interval (t_{LZ}) between comparisons of the actual value with the switching and signalling ranges is computed as follows:

  $t_{LZ\ max.} = t_{ka1\ max.} + t_{ka2\ max.} + 2 \cdot t_{kom\ max.}$

  $t_{ka1\ max.}$ = Maximum processing time for channel 1
  $t_{ka2\ max.}$ = Maximum processing time for channel 2
  $t_{kom\ max.}$ = Maximum time needed for the data interchange

  In Chapter 12 (”Response Times”) you will find a list of processing times to help you compute the suitable distance values for your application. Assuming the maximum possible processing times for channel 1 and channel 2 and the maximum amount of time needed for the data interchange, $t_{LZ\ max.}$ computes to 7.5 ms.

- Tolerance of the contactor dropout times
- Tolerance of the effect of deceleration
- Mechanical influences (such as a change in frictional conditions)

Note

Traversing of the zones switching point BEE1 - switching point BEE2, switching point BEE2 - signalling point BEE3 and the overtravel within the target range should be monitored by watchdog timers.
The IP responses listed in table 10-13 are initiated only once per selected position.

Transferring the distance values with the configuring FB
The distance values are initially transferred to the IP 240 when you configure the channel. Before invoking FB 167, you must enter the distance values in the data block.
The distance value in data words 50 and 51 is for range BEE1,
the distance value in data words 52 and 53 for range BEE2,
and the distance value in data words 54 and 55 for range BEE3.

Permissible range of values:
- for a linear axis : 1 to 999,999
- for a rotary axis : 1 to 0.5·[final value for the rotary axis], but not exceeding 999,999

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 50/52/54	0	0	0	0	0	0	0	0	0				0			
DR	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
50/52/54	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DL 51/53/55	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			
DR																

You can change the distance values after configuring by transferring new values.

> **Note**
>
> If you have chosen BCD representation for the position values and for the distance values, the IP 240 carries out format conversions following transfer of these data. These conversions on-load the firmware cycle. Note that this also affects the response time of the other channel.

10.9 Monitoring Signal Acquisition (IMP)

In positioning mode, the IP 240 can monitor signal acquisition as follows:

Wirebreak/short-circuit in the encoder lines
Wirebreak/short-circuit monitoring is possible only for symmetrical incremental encoders. Monitoring is activated automatically when you set switchbank S5 or S6 for symmetrical encoders (Section 5.3.1). The IP monitors for wirebreak/short-circuit by comparing encoder pulse trains A, B and Z with their inverse signals.
If an error is detected, the IP 240 sets status bit **DRBR** (wirebreak). This bit remains set on the IP until the problem has been rectified and the DRBR bit has been read out at least once over the status area or interrupt request bytes (Section 10.17).

Zero mark monitoring
Zero mark monitoring is used to detect spurious or missing pulses, and is possible only when
- the number of encoder pulses between two zero marks (Z signals) is divisible by 4 or 5 without a remainder,
- the timing of the zero mark signal satisfies the conditions discussed in Section 13.1 ”Signal Forms and Timing Requirements for Incremental Encoders” and
- a reference point approach was terminated with synchronization.

If the IP 240 discovers that the number of pulses between two Z signals is not divisible by 4 or 5 without a remainder, it sets status bit **NPUE** (zero point monitoring).
Status bit NPUE remains set on the IP until it has been read out over the status area or interrupt request bytes (Section 10.17).

Initializing zero point monitoring
When you configure the channel, you must indicate whether or not you want zero mark monitoring, and which encoder you are using, by initializing FB 167's IMP parameter accordingly.

	:	JU FB 167		
NAME	:	STRU.POS		
	:			
	:			
IMP	:	KF x	x=0	No zero mark monitoring
			x=10	The number of encoder pulses between two zero marks is divisible by 5 without a remainder.
			x=16	The number of encoder pulses between two zero marks is divisible by 4 without a remainder.

Zero mark monitoring must be deactivated when
- the encoder cannot satisfy the timing requirements for the reference signal
- the number of pulses between two Z signals is divisible by neither 4 nor 5.

Note

The IP checks for a wirebreak/zero mark error in every module firmware cycle. In the event of an error,
- the outputs are disabled and the positioning procedure currently in progress is interrupted,
- the position number is deactivated,
- status bits BEE1, BEE2, BEE3 and RICH are set to ”1”,
- status bit SYNC is set to ”0”.

The actual value must then be resynchronized.

10.10 Initializing the Parameters for Interrupt Generation (PRA1, PRA2, ABIT)

The following status bits have interrupt capability, and can trigger an interrupt on the S5 CPU when they go to ”1” or ”0”. The associated interrupt bit is also set in the interrupt request bytes.

Table 10-14. Status Bits with Interrupt Capability and the Associated Interrupt Bits

Status bit	Interrupt bit	Function
BEE1	BE1	Range BEE1 entered
BEE2	BE2	Range BEE2 entered
BEE3	BE3	Range BEE3 entered
ZBEV	ZBV	Target range exited
RIUM	RIU	Reversal point reached

Status bit	Interrupt bit	Function
MESE	MES	Final value stored
UEBS	UBS	Final value overwritten
UEBL	UEB	Overrange
DRBR	DRB	Wirebreak
NPUE	NPU	Zero mark error

:positive edge triggers interrupt :negative edge triggers interrupt

> **Note**
>
> The interrupts for actual value-dependent status bits BEE1 to 3, ZBEV and RIUM are generated only once for each position selected.
> If, for example, range BEE1 is exited following an interrupt and subsequently reentered, no new BE1 interrupt is generated.
> New interrupts are possible only when a position number is reselected.

Initializing the parameters for interrupt generation
When you configure the channel, you can specify the status bits that are to trigger an interrupt in parameters **PRA1** and **PRA2**.

```
        :  JU FB 167
NAME    :  STRU.POS
        :                          Assigned
        :                          to status bit
PRA1    :  KM    Bit 0               BEE1
        :        Bit 1               BEE2
        :        Bit 2               BEE3
        :        Bit 3               MESE
```

```
        :  JU FB 167
NAME    :  STRU.POS
        :                          Assigned
        :                          to status bit
PRA2    :  KM    Bit 0               UEBL
        :        Bit 1               NPUE
        :        Bit 2               DRBR
        :        Bit 3               UEBS
        :        Bit 4               ZBEV
        :        Bit 5               RIUM
```

The bits that are to generate an interrupt must be ”1”.

How an interrupt is generated depends on the PLC in which the IP 240 is used (Section 5.1).

Following an interrupt, the interrupt request bytes must be read out from the IP
(Section 10.17).

When using an S5-150U or S5-155U (150 mode), note that the ABIT parameter must also be initialized. In these programmable controllers, an interrupt service OB is invoked at the next block boundary when the associated bit in PY 0 (I/O byte 0) changes its signal state. By initializing the **ABIT** parameter accordingly, you can indicate whether the interrupt service OB is to be invoked every time the signal state of the interrupt bit changes, or only when the bit goes from ”0” to ”1”.

Initializing the ABIT parameter:

	:	JU FB 167			
NAME	:	STRU.POS			
	:				
	:				
ABIT	:	Ky x,y	x>0	:	The interrupt service OB is to be invoked on every signal change
			x=0	:	The interrupt service OB is to be invoked only on a signal change from ”0” to ”1”
			y=0 to 7	:	y is the number of the bit in PY 0 that was set on switchbank S1

Masking interrupts
You can mask all channel bits with interrupt capability by setting control bit **AMSK** (mask interrupts) to ”1” and transferring it to the IP 240. Masked interrupts do not trigger an interrupt request and are not stored in the interrupt request bytes, i.e. they are lost.
Refer to Section 10.13.4 for information on how to transfer the control bits to the IP 240.

10.11 Error Processing after Configuring

If an error occurs during configuring,
- configuring of the channel is aborted and
- the error is flagged in the PAFE byte (Section 6.4).

Errors in FB parameters are detected by the FB, and are described in more detail in DW 13 of the specified data block.
Hardware, communications and data errors are flagged by the IP 240, and are read out from the IP automatically by FB 167 and entered in KH format in data words 8 to 10 of the data block. Data word 10 always contains the code of the last error detected.
After the error flags have been processed, you must erase the contents of data words 8 to 10 and DW 13 via the STEP 5 program.

Old communications and data errors are cleared by the configuring FB.

You will find a list of all error codes in Chapter 14.

> **Note**
>
> The PAFE byte should be evaluated after every FB 167 call.

Table 10-15. Contents of Data Words 8 to 10

Data byte	Bit 7	6	5	4	3	2	1	0	Description
DL 8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 3
DR 8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 3
DL 9	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 2
DR 9	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 2
DL 10	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 1
DR 10	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 1

10.12 Controlling the IP and Evaluating IP Data

Sections 10.13 to 10.21 describe the available options for IP control following configuring, and tell you

- what data is made available by the IP 240 and
- how this data can be read out from the IP and evaluated.

After configuring, you can either use control FB 168 for data interchange between the S5 CPU and the IP 240, or you can program direct data interchange between CPU and IP yourself.

Data interchange using control function block FB 168
As does the configuring FB, control FB 168 uses a data block (DB) for data interchange between S5 CPU and IP 240.
In the following sections, you will find information on

- the data words in which you must enter new data for a Write,
- the data words in which data read out from the IP 240 is entered and
- how you must initialize the FB so that it will transfer the new data.

In Section 10.23.1 you will find a summary of the contents of the data block, and in Section 10.23.3 a summary of the parameters for control FB 168.

Direct data interchange
Direct data interchange means that you can transfer data directly to or read data directly from the IP 240. A 16-byte address space is provided for direct data interchange. By specifying a job number, you tell the IP 240 which job it is to execute.
In the following sections, you will find information on

- the job numbers you must use,
- the contents of the transfer buffer for the various jobs and
- the offset under which the various bytes can be read or written. The absolute address is a composite of the offset and the module start address.

Chapter 11 ”Direct Data Interchange with the IP 240” provides a detailed description of direct data interchange.

10.13 Methods of Synchronization

Positioning is possible with the IP 240 only when the actual value has been synchronized. Three methods of synchronization are available for this purpose:

- Reference point approach
  A reference point approach synchronizes the actual value to a fixed point in the traversing range.

- Software-controlled synchronization
  The actual value is synchronized every time a control bit with a value of ”1” is transferred.

- Synchronization with an external control signal
  The actual value is synchronized every time there is a positive signal edge at the IP 240's IN input, and the current actual value is stored on every negative signal edge at this input. This value can be read out as final value (e.g. of a length measurement).

You select the synchronization method you want to use via a control bit. It is thus possible to specify different methods successively.
Synchronization sets the actual value to the value of the zero offset last transferred (NVER), irrespective of whether the zero offset in question is an additive or relative zero offset.

10.13.1 Reference Point Approach

A reference point approach synchronizes the measuring system to a reference point in the traversing range. The location of the reference point is determined by the first zero mark signal (Z signal) from the incremental encoder that follows a preliminary contact signal.
To generate the **preliminary contact signal**, you must insert a bounce-free switching element in the traversing range and connect it to the channel's **IN input**. Because the IN signal may already be active at the start of the reference point approach, it is possible to use an existing limit switch as sensor for the preliminary contact signal.
The encoder used must supply at least one zero mark signal per revolution, and must meet the timing requirements discussed in Section 13.1.2.
If the channel was configured without backlash compensation, synchronization is possible in both directions of travel. If the channel was configured with backlash compensation, the actual value is synchronized only when the preliminary contact is exited with ascending actual value (positive direction of travel).

> **Note**
>
> You must make sure that synchronization always takes place at the same zero mark position by selecting the traversing speed during reference point approach and aligning the negative preliminary contact edge between two zero marks. Moreover, the direction of travel may not be changed after the negative preliminary contact edge.
>
> During reference point approach, the Z signal is evaluated while A=1 and B=1. This state may occur only once for the duration of the Z signal (Z=1).
>
> You will find a list of timing requirements in Chapter 13 ”Encoder Signals”.

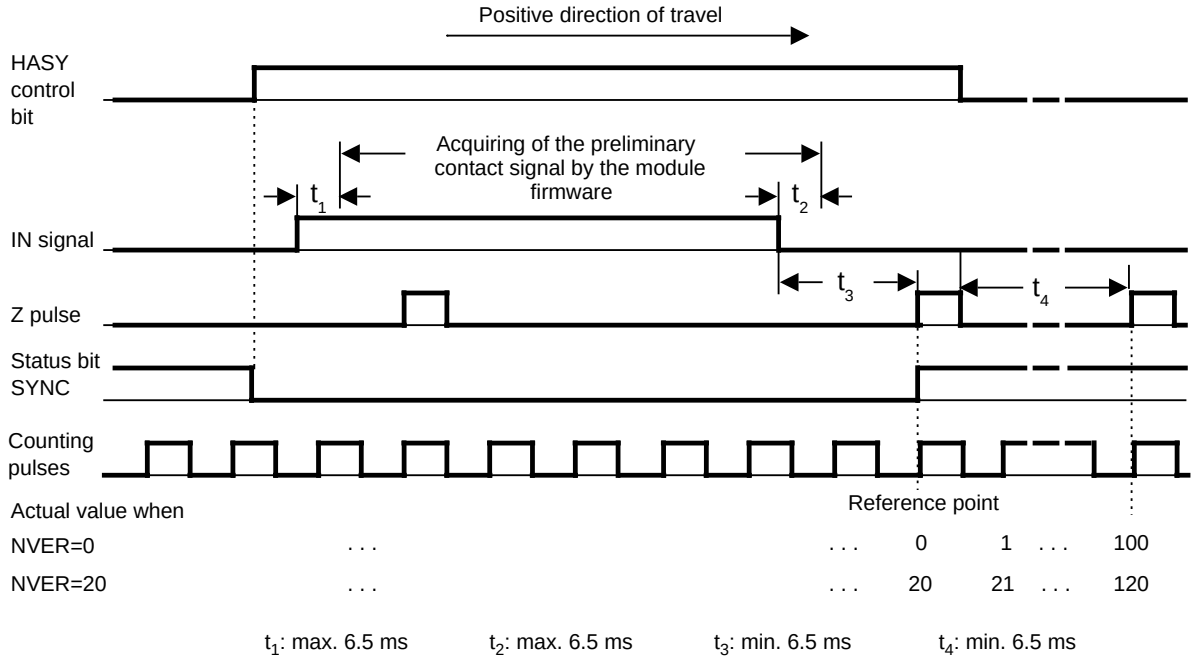


Fig. 10-22. Location of the Reference Point on Reference Point Approach

As the preliminary contact signal is evaluated over the IP 240 module firmware, care must be taken that acquisition of the signal edges is delayed by t_1 and t_2. Moreover, time value t_3 must be carefully observed.
After synchronization, the next zero mark must not occur for at least 6.5 ms (t_4). If this is not observed, the actual value may be synchronized again.

Using the control bits for reference point approach

- Control bit **HASY** (**HA**rdware-controlled **SY**nchronization) is used to select a reference point approach.
  When HASY = 1 the channel is set to ”reference point approach” mode
  When HASY = 0 the reference point approach can be exited or aborted following synchronization

- The **FREI** control bit is used to enable the IP outputs at a supraordinate level
  When FREI = 0 the outputs for the channel are disabled
  When FREI = 1 the outputs for the channel are enabled

- The **HAND** control bit is used to specify whether the IP outputs are to be controlled by the IP 240 module firmware during reference point approach or whether the outputs are to be switched as prescribed by the S5 CPU.
  When HAND = 0 the channel's outputs are controlled by the module firmware

  When HAND = 1 the outputs are switched as prescribed by control bits DA1S and DA2S

- Control bits **DA1S** and **DA2S** are used to control switching of the IP outputs.
  When DAnS = 0 output Dn is reset
  When DAnS = 1 output Dn is set
  The permissible combinations of DA1S and DA2S depend on configuring parameter DAV, and are checked by the module firmware.

If you configured the channel with DAV=2 (the IP controls the direction of travel during positioning) and want to pass control of the channel's outputs to the module firmware (HAND = 0) during reference point approach, you must specify the direction of travel for reference point approach via DA1S and DA2S.

In the following flow diagrams, it has been assumed that the IP outputs will be controlled by the module firmware following selection of reference point approach, and that they have been enabled. For this purpose, the control bits must be transferred to the IP as follows.

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	1	0/1	1/0	0	1

Sequence of a reference point approach

Approaching the starting point

As the current position is not known following ”power-up”, it is necessary to first approach a starting position. All outputs for drive control must be initialized via the S5 CPU. The IP outputs must be controlled via the bits HAND=1, FREI=1 and DAnS (n=1 or 2).

Approaching the reference point

1) Check to make sure that the IP outputs are disabled.
   You can select a reference point approach only when the IP outputs are disabled.
   You can check the state of the outputs by reading the status area and evaluating bits DA1 and DA2 (Section 10.16).
   To disable the outputs, FREI must be transferred with ”0” to the IP 240.

2) Select reference point approach, specify the direction of travel and enable the IP outputs.
   Set HASY to ”1” to select reference point approach.
   a) If the IP outputs are to be controlled via the S5 CPU (**HAND**=1), the HASY bit must first be transferred to the IP 240 without enabling the outputs.

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	1	x	x	1	0

FREI must then be set to ”1”.

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	1	x	x	1	1

x) depending on the DAV parameter

b) If the IP outputs are to be controlled by the module firmware (**HAND=0**), they can be enabled immediately (FREI=1).
If the IP 240 controls the direction of travel during positioning (DAV=2), you must also set control bit DA1S or DA2S for reference point approach to specify which input is to be set.

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	1	0/1	1/0	0	1

Following transfer of the HASY control bit,
- the SYNC bit is set to ”0” and
- range bits BEE1 to 3 and direction bit RICH are set to ”1”, as the last position number selected was invalid. Position number ”255” is always returned (Section 10.16).

The reference point approach is started when the outputs are enabled.

3) When the preliminary contact is reached, bit BEE1 is set to ”0” and the traversing speed switched to creep speed.
If the IP 240 controls the traversing speed (DAV=0 or 1, HAND=0), the speed is always switched to creep when the preliminary contact is reached.
If the IP 240 controls the direction of travel, you can monitor reaching of the preliminary contact by evaluating status bit BEE1 or interrupt bit BE1.

4) When the preliminary contact is exited, status bit BEE1 is set back to ”1”.

5) Synchronization is initiated by the first zero mark signal that follows the preliminary contact signal.
- The IP output still active is reset (HAND=0)
- Status bit SYNC is set.
- The actual value is set to the most recently specified zero offset value.
- Status bit BEE2 is set to ”0” and interrupt BE2 generated.

6) Reference point approach is exited.
To quit reference point approach, set HASY to ”0” and transfer it to the IP 240. The first position number may also be selected (Section 10.14.1). Status bit BEE2 is set to ”1”.

7) Block outputs
For blocking the IP outputs, FREI is to be set to ”0” and transferred to the IP. In doing so, the first position number may also be selected. (Section 10.14.1).

Note

If the HASY and FREI control bits are set to ”0” while quitting the reference point approach, zero mark monitoring (Section 10.9) is **not** started.

Switching the IP outputs during reference point approach (HAND=0)
The switching performance of the IP outputs specified when the channel was configured is taken into account during reference point approach.

a) DAV=0 (switch outputs separately)
After the outputs have been enabled (FREI=1), IP output D1 is set.
When the preliminary contact signal is reached (positive edge at the IN input), output D1 is reset and output D2 set. D2 is reset when the reference point is reached.

b) DAV=1 (switch outputs collectively)
After the outputs have been enabled, both D1 and D2 are set.
When the preliminary contact signal is reached, output D1 is reset; output D2 is reset when the reference point is reached.

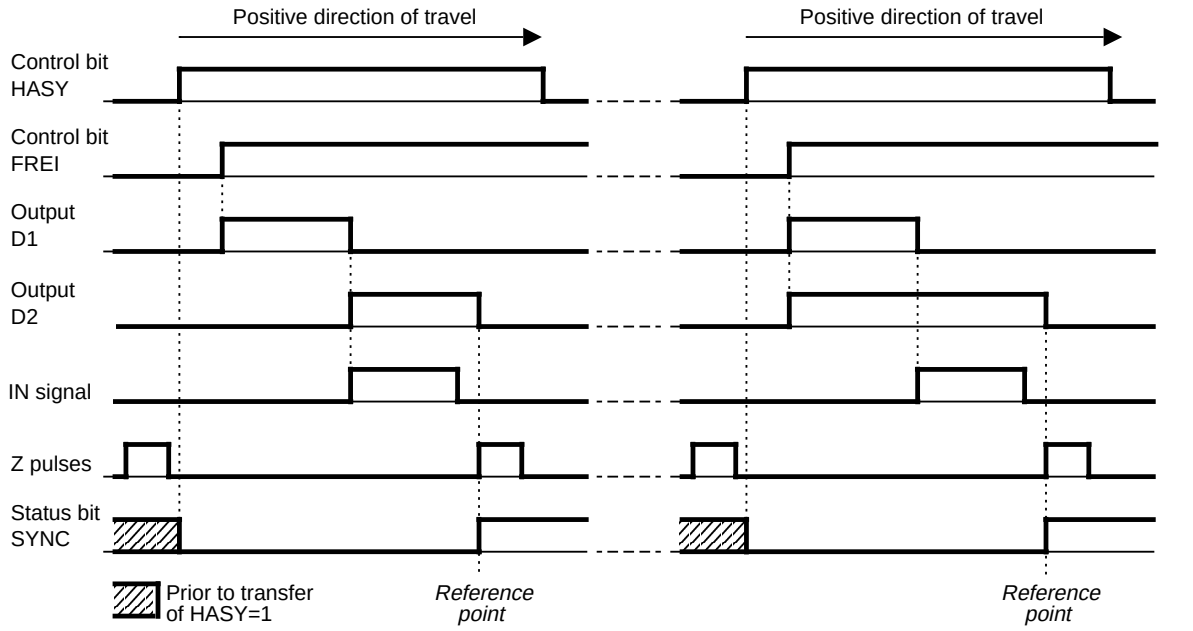


Fig. 10-23a. Switching of the IP Outputs during Reference Point Approach when DAV=0

Fig. 10-23b. Switching of the IP Outputs during Reference Point Approach when DAV=1

Note

Only output D2 is set if the IN signal is already active at the start of reference point approach.

c) DAV=2
After the outputs have been enabled, the IP output specified by setting control bit DA1S **or** DA2S is set.
The output is reset when the reference point is reached.

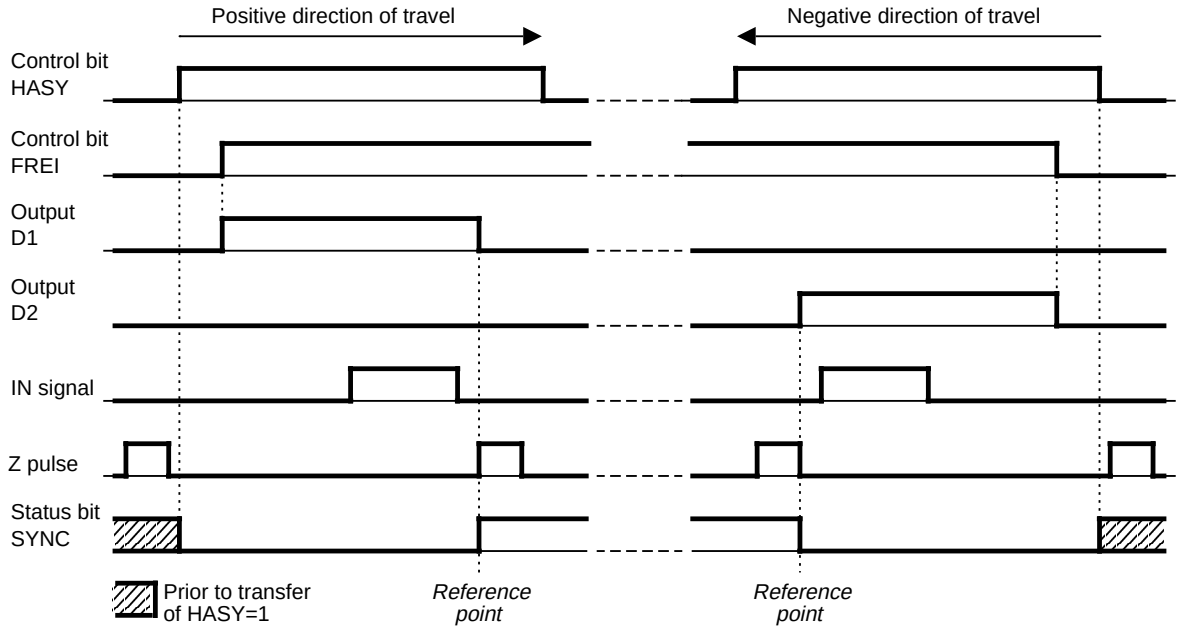


Fig. 10-24. Switching of the IP Outputs during Reference Point Approach when DAV=2

Backlash compensation during reference point approach (LOSE=1)
If you have configured the channel for backlash compensation, synchronization is possible in a **positive** direction of travel only (ascending actual value). Decisive for evaluation of the direction is the instant at which the preliminary contact signal is exited (negative edge of the IN signal).
If the preliminary contact signal was exited in a **negative** direction, the encoder's next zero mark signal has the following effect:

- The actual value is reset
- Synchronization bit SYNC is **not** set
- The IP output is **not** reset

To reverse the direction, the drive must be stopped over the S5 CPU. To do this, transfer control bit FREI=0 to the IP 240. The reference point approach must then be repeated.

Note

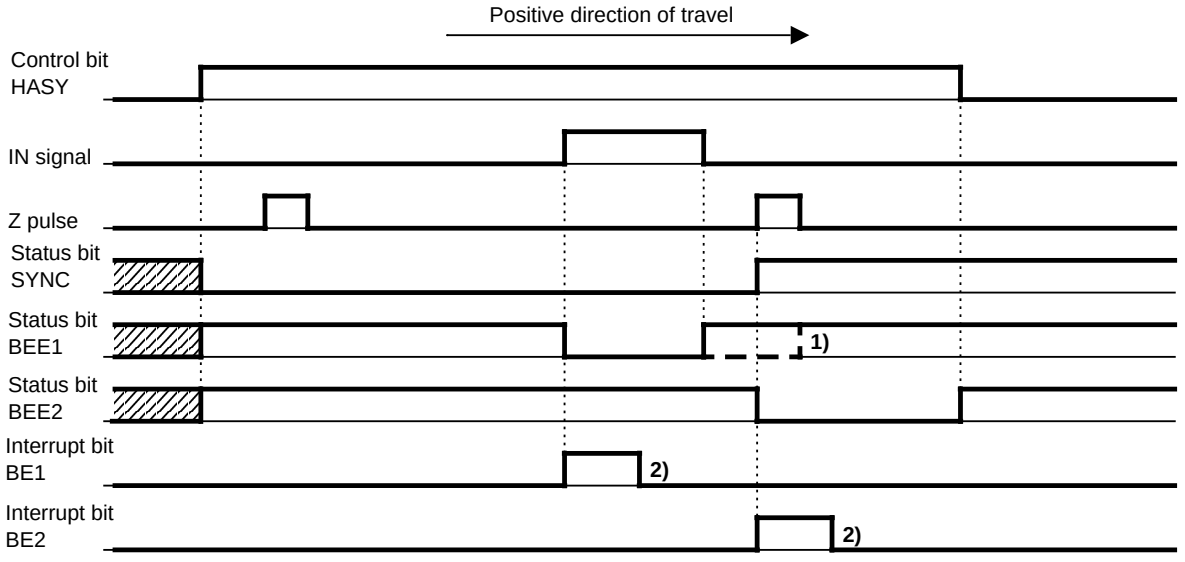
In order to ensure that synchronization is always carried out at the same place, the direction of travel may not be changed following a negative edge of the preliminary contact signal.

Status of range bits BEE1, BEE2 and BEE3 during reference point approach
When reference point approach is selected, all three range bits (BEE1, BEE2 and BEE3) are set to ”1”.
Bit BEE1 is set to ”0” when the preliminary contact is reached. It remains at ”0” until the preliminary contact is exited and the status area on the IP 240 has been read at least once. You can control the switch to creep speed by evaluating status bit BEE1 (Section 10.16).
Bit BEE2 is set to ”0” when the reference point is reached, and remains at ”0” until the reference point approach is exited by transferring control bit HASY=0.

Interrupts during reference point approach
When you configure the channel, you can specify whether status bit BEE1 and/or BEE2 is/are to have interrupt capability.
The following information is provided on interrupts:

BE1=1 The preliminary contact was reached and the speed must be switched to creep.
If the preliminary contact signal was already active at the start of reference point approach, interrupt BE1 is generated immediately.
BE2=1 The reference point was reached.

Refer to Section 10.17 ”Reading the Interrupt Request Bytes” for information on how to read out the interrupt bits from the IP 240.



1) Is set to ”1” following reading of the status area
2) Is reset following reading of the interrupt request bytes

Fig. 10-25. Range Bits BEE1 to 2 and Interrupt Bits BE1 to 2 during Reference Point Approach

Note

If the channel was structured for backlash compensation, the next Z signal from the encoder following exiting of the preliminary contact signal in a negative direction does not set status bit BEE2 to ”0” and does not trigger interrupt BE2.

Interrupting a reference point approach
You can interrupt a reference point approach by transferring
- control bit HASY = 0 or
- control bit FREI = 0 to the IP 240.

When the reference point approach is interrupted with HASY=0 and FREI=1, the IP outputs are disabled only when they are are under IP 240 module firmware control during reference point approach (HAND=0).

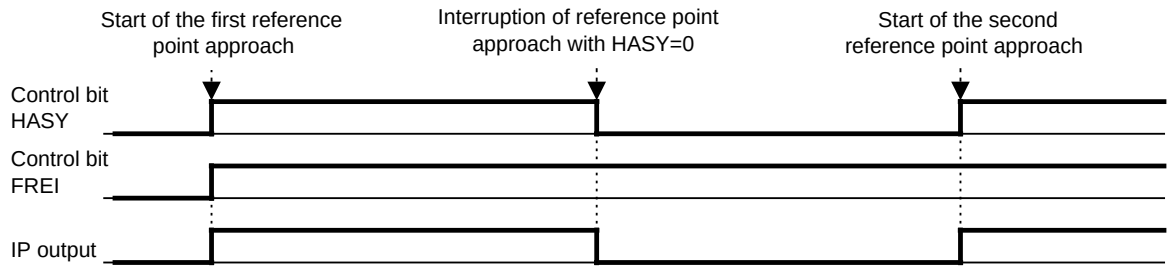


Fig. 10-26. Interrupting a Reference Point Approach with HASY=0 (HAND=0)

When a reference point approach is interrupted with FREI=0, the IP outputs are always disabled. Before a new reference point approach can be started, the old reference point approach must first be deselected with HASY=0. HASY=0 can be transferred together with FREI=0.

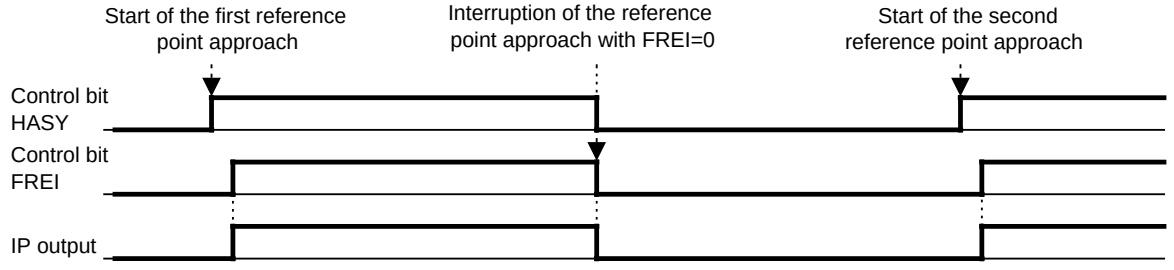


Fig. 10-27. Interrupting a Reference Point Approach with FREI=0

10.13.2 Software-Controlled Synchronization

Synchronization can be carried out at any point in the traversing range by transferring a control bit with a value of ”1”. This reactivates the position last selected. Software-controlled synchronization is also possible when the channel's outputs are set.

The SOSY control bit
Each time SOSY=1 is transferred, the IP 240 initiates software-controlled synchronization. This means that
- the actual value is set to the value of the zero offset last transferred
- synchronization bit SYNC is set and
- the position last transferred is immediately reactivated. On the basis of the current actual value,
  - status bits BEE1 to 3 and RICH are updated,
  - the enabled outputs are set and
  - the configured interrupts are generated.

The new position number can be transferred to the IP 240 together with SOSY=1. Refer to Section 10.14.1 for information on how to select a position number.
If there is to be no software-controlled synchronization, you must set SOSY to ”0” prior to the next transfer of the control bits.

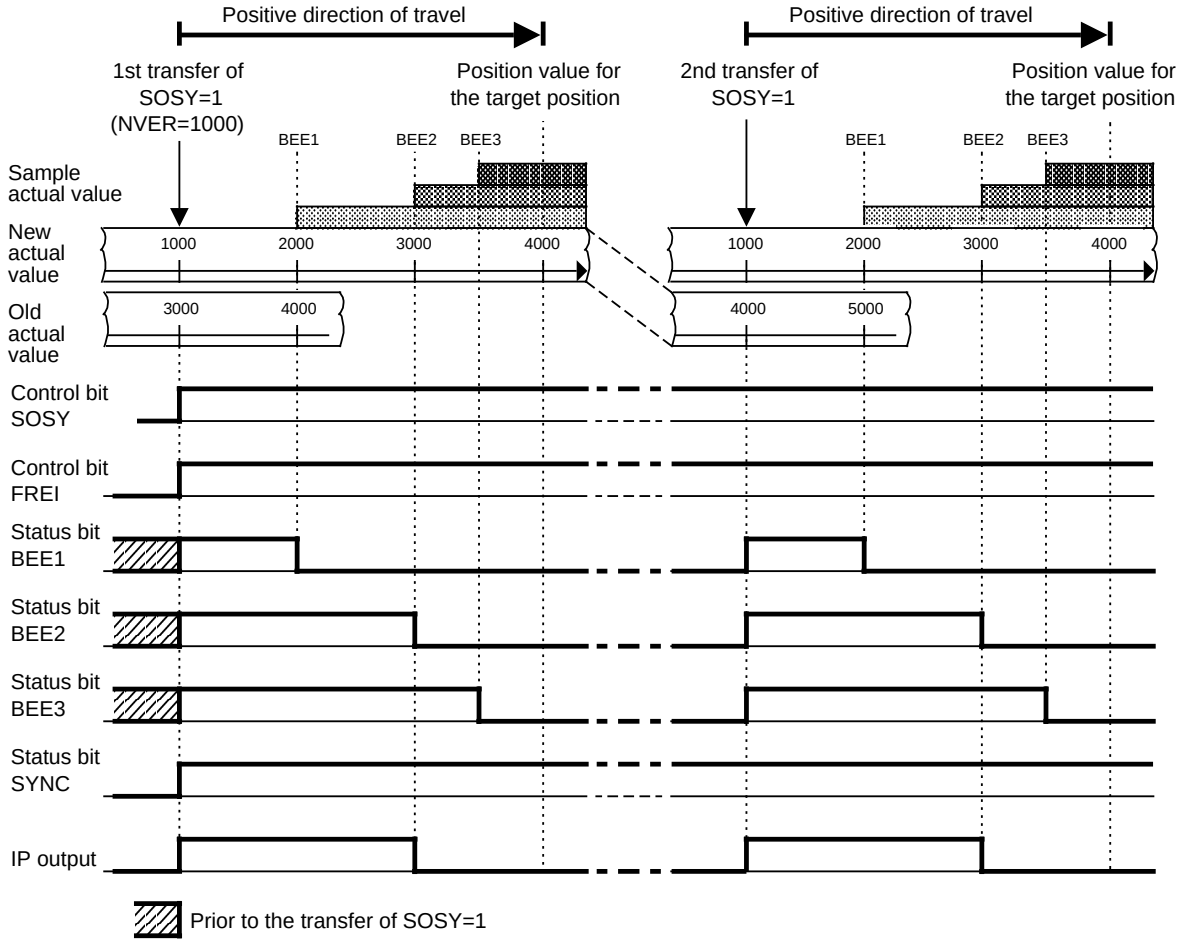


Fig. 10-28. Software-Controlled Synchronization

Explanation: A zero offset (NVER) of 1000 is initialized prior to the first transfer of SOSY=1.
A position number with an associated position value of 4000 is transferred together with SOSY=1.
The actual value prior to the first software-controlled synchronization was 3000, the new actual value is 1000.
No new position number is selected on the second transfer of SOSY=1, so that the ”old” position number (position value=4000) is reactivated.

Warning

As software-controlled synchronization is also permitted when the IP outputs are set and the selected position goes into force immediately, it is possible that the states of the outputs could change instantaneously, causing a short-term overlap.

Following transfer of SOSY=1, the actual value is reset within max. 5 ms.

10.13.3 Synchronization with an External Control Signal

When synchronization with an external control signal, referred to from here on as ”cyclic synchronization”, is used, the IP 240 evaluates the edge change at the IN input.
On a positive signal edge (signal change from 0 to 1) at this input, the actual value is set to the value of the zero offset and the position last selected reactivated.
On a negative signal edge (signal change from 1 to 0) at this input, the current actual value is stored in a final value register.
Since normal actual value acquisition takes place in parallel to the evaluation of the edge change at the IN input, positioning is also possible in this synchronization mode.

The ZYSY control bit
Cyclic synchronization is selected via the **ZYSY** control bit. This bit is evaluated on an edge-triggered basis.
The first time ZYSY=1 is transferred,
- the SYNC bit is reset.
- range bits BEE1 to 3 and direction bit RICH are set to ”1”, as the position number last selected was invalidated, and
- the channel's outputs are disabled.

  When you select cyclic synchronization you can also specify a new position number; the new position number, however, does not go into force until there is a positive signal edge at the IN input.
  Refer to Section 10.14.1 for information on selecting a position number.

To exit cyclic synchronization, you must transfer ZYSY=0 to the IP 240. This does not affect any synchronization currently in progress.

Evaluating the IN signal
When you select cyclic synchronization, a **positive-going** edge at the IN input initiates the following on the IP 240:
- The actual value is set to the value of the zero offset
- Synchronization bit SYNC is set
- The position last transferred is immediately reactivated and
- In dependence on the current actual value,
  - range bits BEE1 to 3 and RICH are updated,
  - the enabled outputs are set and
  - the interrupts configured for the active position are generated.

The following steps are initiated on a **negative-going** signal edge at the IN input:
- The current actual value is stored in a final value register.
  You can read this final value from the IP together with the actual value (Section 10.16).
- Status bit **MESE** (measuring terminated) is set to show that the final value was stored.
- The interrupt allocated to status bit MESE is generated and the MES bit set in the interrupt request bytes.
- A check is made to see whether or not the final value has been read out from the IP.
  If it has not, status bit **UEBS** (Overwrite) is set.
- The interrupt allocated to status bit UEBS is generated and the UBS bit set in the interrupt request bytes.

> **Note**
>
> If the IN signal was already active when cyclic synchronization was selected, no synchronization takes place. The subsequent negative-going edge is not evaluated.

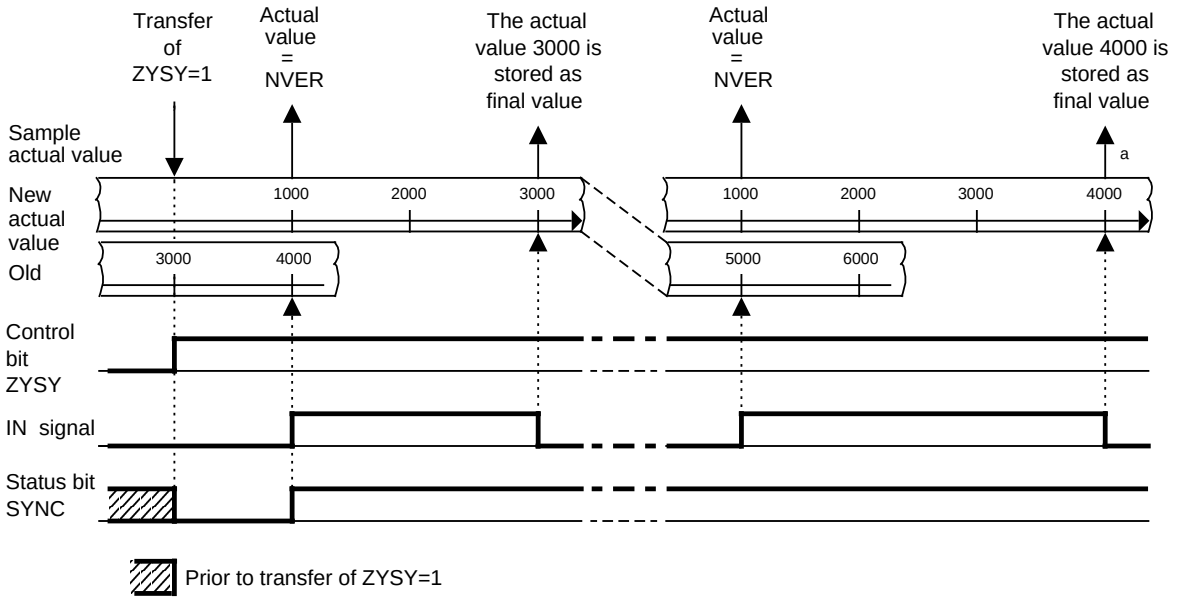


Fig. 10-29. Synchronization with an External Control Signal at the IN Input

Explanation: A zero offset (NVER) of 1000 has been set prior to transfer of ZYSY=1.
The positive-going edge of the synchronization signal at the IN input sets the actual value to 1000.

a The current actual value (3000 or 4000) is stored as final value on the negative-going edge.
If actual value 3000 is not read prior to the second negative-going signal edge at the IN input, status bit UEBS is set and interrupt UBS generated, if configured.

Note

As the IN signal is evaluated by the module firmware, note that an entire firmware cycle may lie between the occurrence and the detection of an edge. The counting procedure is thus started with a delay of t_1 (Fig. 10-30) and terminated with a delay of t_2, resulting in an inaccuracy of the acquired counting pulses between positive-going and negative-going IN signal edge of max. 7.5 ms when the direction of counting is not changed.
Refer to Section 13.2 for a diagram of timing requirements.

The IN signal may not be active until 5 ms after the initial transfer of ZYSY=1.

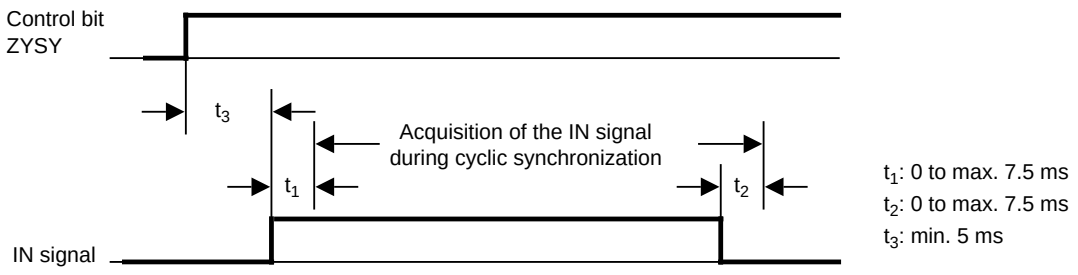


Fig. 10-30. Acquisition of the IN Signal during Cyclic Synchronization

Warning

Cyclic synchronization is also allowed when the IP outputs are set. The position transferred goes into force immediately on an IN signal. The states of the outputs may thus change instantaneously, causing a short-term overlap.
A bounce-free switching element must be used to generate the IN signal.

10.13.4 Transferring Control Bits to Select a Synchronization Mode

Note the following when initializing the control bits to select a synchronization mode:
- You can select only one synchronization mode at a time.
- You must take configuring parameter DAV into account when initializing control bits DA1S and DA2S. The following bit combinations are permitted:

DAV =0	DA1S	DA2S	DA1S	DA2S	DAV =1	DA1S	DA2S	DA1S	DA2S	DAV =2	DA1S	DA2S	DA1S	DA2S
	1	0	0	1		1	1	0	1		1	0	0	1

When transferring control bits for selecting a reference point approach, note that
- you may not transfer a position number with the control bits and
- the IP outputs must be disabled.

The following error flags are set when illegal bit combinations are transferred to the IP 240. Such illegal bit combinations are rejected.

Table 10-16. Contents of the DB and the Transfer Buffer for the Transfer of Control Bits

Data byte Data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 36	AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI	2	Control bits
DR 36	0	. . .		0	0	. . .		0	3	

Tranfer of control bits without position number	
with control FB 168	**in direct data interchange**
The new control bits must be entered in DL 36 in the data block. Control FB 168 must be initialized as follows: : JU FB 168 NAME : STEU.POS : FKT : 20,0	You must specify the following job numbers to transfer the control bits: • For channel 1: $1A_H$ • For channel 2: $2A_H$ To write the control bits, you need only transfer the byte with offset 2. If you also write the byte with offset 3, you must initialize this byte to ”0”.

10.14 Selecting a Position

Positioning is started by selecting a position. The IP 240 uses the position value for the position selected as the new setpoint, and computes the locations of ranges BEE1 to 3 from the specified distance values.

You can define the new target position
- by selecting the number of a position (1 to 254) whose position value has been stored on the IP 240 or
- by specifying a position value for position 0.

10.14.1 Selecting a Stored Position Between 1 and 254

You stored the position data for positions 1 to 254 on the IP 240 during configuring. To select a stored position, you must transfer the number of that position and the control bits to the IP.

Table 10-17. Contents of the DB and the Transfer Buffer for Transferring the Control Bits and the Position Number

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 35	0	...		0	0	...		0	0	
DR 35	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	New position to be approached (1 to 254)
DL 36	AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI	2	Control bits
DR 36	0	...		0	0	...		0	3	

Transferring the control bits and the position number for positions 1 to 254	
with control FB 168	**in direct data interchange**
You must enter the new control bits in DL 36 in the data block. Specify the new position number as y value in the FKT parameter when you call FB 168. The FB enters this value in the data block in DR 35. Initialize control FB 168 as follows: : JU FB 168 NAME : STEU.POS : FKT : 21,y y=new position number 1 to 254	You must specify one of the following job numbers to transfer the control bits and the new position number: • For channel 1: $1A_H$ • For channel 2: $2A_H$. If the bytes with offset 0 and 3 are also to be transferred, they must first be initialized to ”0”.

If you transfer position number 255, the current position number is retained. An error is flagged if you specify position number ”0”.

Note

The IP 240 accepts the specified position number only when control bit HAND is not set. In addition,

- status bit SYNC must be set and the specified channel's outputs disabled or
- SOSY=1 or ZYSY=1 (if ZYSY=1 for the **first time**) must be transferred together with the position number.

You can set and transfer the following control bits together with the position number:

- AMSK to mask all interrupts,
- ZYSY **or** SOSY to select the synchronization mode,
- FREI to enable the outputs.

If you do not transfer the control bits in a direct data interchange with the IP 240, the old control bits are reevaluated.

Sequence for selecting a position between 1 and 254

1) Check to make sure that the IP outputs are disabled
   A position number can be transferred only when the IP outputs are disabled.
   To check the state of the outputs, you must read the status area and evaluate bits DA1 and DA2 (Section 10.16 ”Reading and Evaluating the IP Status Information”).

2) Disable the outputs
   You can disable the IP outputs by initializing the FREI bit to ”0”.

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	0	0	0	0

3) Transfer the new position number and the control bits
   After transferring the new position number with FREI=0, you can determine the relation of the current actual value to the new position value by reading the status area and evaluating status bits BEE1 to 3 and RICH.

4) a) Enable IP outputs with HAND=0
   (IP outputs under module firmware control)

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	0	0	0	1

   b) Enable outputs with HAND=1
   (IP outputs controlled by DA1S and DA2S via S5 CPU)

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	X	X	1	1

x) depending on the DAV parameter

If it is necessary to disable the IP outputs, you can do so by transferring FREI=0 and, at the same time, specify the new position number (thus combining steps 2 and 3).

If it is not necessary to disable the IP outputs, you can omit step 2 and transfer the new position number together with control bits FREI=1 and HAND=0 (thus combining steps 3 and 4). In this case, however, the module **sets** the outputs **immediately** in dependence on the actual value.

If you want to control the IP outputs over the S5 CPU, you must always initialize control bit FREI to 1 and control bit HAND to 1 every time you write the new position number.

10.14.2 Selecting Position 0

The data for position 0 is not stored on the IP 240.
To select position 0, you must transfer the new position value. The IP 240 interprets this value as the new target position when the actual value was previously synchronized (status bit SYNC=1). You can also select position 0 when the IP outputs are set, thus making it possible to modify the positioning procedure currently in progress without resetting the IP outputs.

> **Note**
>
> Since position 0 can also be selected when the IP outputs are set, instantaneous switching of the outputs is possible.

Together with the position value, you can also
- specify distance values for ranges BEE1 to 3
- set bit GAUE (D44/8) to indicate that the distance values stored on the IP for positions 1 to 254 are to be used. In this case, any newly specified distance values are checked, but otherwise ignored.

Valid position data for position 0
The position value and the distance values may be assigned the following values:

Range of values for	Range limits	Number format	
		Binary	BCD
the position value for a linear axis	-9,999,999 to +9,999,999	•	•
the position value for a rotary axis	0 to [final value for rotary axis - 1]	•	•
the distance values for ranges BEE1 and BEE2 (additional values for rotary axis)	0 to 999,999, (but not exceeding 0,5·[final value for rotary axis])	•	
the distance value for range BEE3 (additional value for rotary axis)	0 to 65,535, (but not exceeding 0,5·[final value for rotary axis])	•	

Note the following when defining the distance values:
Distance value for range BEE1 distance value for range BEE2 distance value for range BEE3

Table 10-18. Contents of the DB and the Transfer Buffer for Writing Position 0

Data byte Data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 37	SE								0	Position value, **in binary**
DR 37	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	1	
DL 38	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2	A negative value is in two's complement representation SE=Sign extension
DR 38	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	3	
DL 37	SG				10^{6}				0	Position value, **in BCD**
DR 37	10^{5}				10^{4}				1	
DL 38	10^{3}				10^{2}				2	"111" must be entered in the high-order nibble of DL 37 (SG) for a negative value.
DR 38	10^{1}				10^{0}				3	
DL 39	0	. . .		0	0	. . .		0	4	Distance value for range BEE1
DR 39	0	. . .		0	2^{19}	2^{18}	2^{17}	2^{16}	5	
DL 40	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	6	
DR 40	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	7	
DL 41	0	. . .		0	0	. . .		0	8	Distance value for range BEE2
DR 41	0	. . .		0	2^{19}	2^{18}	2^{17}	2^{16}	9	
DL 42	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	10	
DR 42	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	11	
DL 43	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	12	Distance value for range BEE3
DR 43	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	13	
DL 44	0	. . .		0	0	0	0	GAUE	14	Control bit GAUE

Transferring the position data for position 0	
with control FB 168	**in direct data interchange**
You must specify one of the following job numbers to transfer the position data for position 0: : JU FB 168 NAME : STEU.POS : FKT : 22,0	You must specify one of the following job numbers to transfer the position data for position 0: • For channel 1: 18_H • For channel 2: 28_H If you also want to transfer the bytes with offset 4 and 8, you must first initialize them to "0".

10.15 Controlling the Digital Outputs During Positioning

You can use IP outputs D1 and D2 to
- change the traversing speed or
- control the direction of travel.

If there are two speeds and two directions of travel, you require two additional PLC digital outputs to implement the additional function. These outputs must be controlled via the S5 CPU. The IP 240 supports this with status bits and interrupts to indicate when the digital outputs have to be set or reset. For this reason, this section is subdivided into two subsections, i.e. ”Controlling the IP Outputs” and ”Controlling the PLC Outputs”.

10.15.1 Controlling the IP Outputs

During positioning, the IP outputs can be set and reset by the IP 240 module firmware or via the S5 CPU over control bits.

Control bits FREI and HAND

Control bit **FREI** is used to enable the specified channel's IP outputs at the supraordinate level. An IP output can be set only when FREI=1 has been transferred to the IP 240. If outputs are set and FREI=0 is transferred, the outputs are reset.

Control bit **HAND** is used to specify whether the IP 240 module firmware is to control the outputs or whether they are to be controlled via the S5 CPU over control bits.

Hand=0 The outputs are to be controlled by the module firmware in dependence on the actual value.

Hand=1 The outputs are to be controlled on the basis of control bits DA1S and DA2S.

Control of the IP outputs by the module firmware (Hand=0)

When Hand=0, the IP 240 controls setting, switching and resetting of the IP outputs. You can initialize the DAV parameter when you structure the channel to define the purpose for which the outputs are to be used. The table below shows the three possible initialization values for the DAV parameter and what these values mean.

• Output active	IP controls the speed DAV=0		IP controls the speed DAV=1		IP controls the direction DAV=2	
	Rapid traverse	Creep speed	Rapid traverse	Creep speed	Positive direction	Negative direction
IP output D1	•		•		•	
IP output D2		•	•	•		•

Control bits for firmware control of the IP outputs

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	0	0	0	1

Controlling the IP outputs via the S5 CPU (HAND=1)
You can define the states which the IP outputs are to assume via the S5 CPU using control bits **DA1S** and **DA2S**.
DAnS=1 Output Dn is to be set.
DAnS=0 Output Dn is to be reset.

The IP 240 accepts HAND=1 only when the IP outputs are disabled (status bits DA1/DA2=0) and no position number is included in the control bit transfer.

Control bits for S5 CPU control of the IP outputs

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	x	x	1	1

x) depending on the DAV parameter

The permissible combinations of DA1S and DA2S depend on the DAV parameter, and are checked by the module firmware. If an illegal bit combination is transferred, an error is flagged and the bit combination rejected.

The following bit combinations are permitted:

DAV =0	DA1S	DA2S	DA1S	DA2S	DAV =1	DA1S	DA2S	DA1S	DA2S	DAV =2	DA1S	DA2S	DA1S	DA2S
	1	0	0	1		1	1	0	1		1	0	0	1

Disabling the IP outputs via control bit FREI (FREI=0)
You can disable the active outputs of a channel by transferring FREI=0 to the IP 240. The outputs remain disabled until you transfer FREI=1. If you interrupt positioning with FREI=0, the outputs are not reenabled until a new position number has been selected. You can transfer the new position number when you

- disable the outputs (FREI=0) or
- reenable the outputs (FREI=1).

Control bits for disabling the IP outputs

AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI
0/1	0	0	0	0/1	0/1	0/1	0

Control FB 168 provides a special function number (FKT=20,1) for disabling the outputs. When this function number is initialized, the FB sets the FREI bit to ”0” in the specified function block, then transfers the control bits to the IP 240.

Note

Starting positioning in the vicinity of range BEE1 or BEE2 may result in a change from rapid traverse to creep speed and in disabling of the outputs under starting conditions. To prevent this, you must evaluate the IP 240 status info (status bits and actual value) following transfer of the target position with FREI=0 before enabling the outputs with FREI=1.

Table 10-19. Contents of the DB and the Transfer Buffer for Transferring the Control Bits

Data byte Data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 36	AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI	2	Control bits
DR 36	0	. . .		0	0	. . .		0	3	

Transfer of the control bits	
with control FB 168	**in direct data interchange**
Yo must enter the new control bits in the data block in DL 36. Initialize the FB 168 as follows to transfer the control bits: : JU FB 168 NAME : STEU.POS : FKT : 20,0	You must specify the following job numbers to transfer the control bits: • For channel 1: $1A_H$ • For channel 2: $2A_H$
Initialize the FB as follows to disable the IP outputs with FREI=0 : JU FB 168 NAME : STEU.POS : FKT : 20,1	If you also want to transfer the byte with offset 3, you first initialize it to ”0”.

10.15.2 Controlling the PLC Outputs

Depending on how the IP 240 was configured, the auxiliary digital outputs are required to change the traversing speed or to control the direction.

The IP 240 provides the following status bits to control these outputs:

- Direction bit RICH:
  RICH=1 Traverse in negative direction (descending actual value).
  RICH=0 Traverse in positive direction (ascending actual value).
- Range bits BEE1, BEE2 and BEE3:
  BEEn=1 The actual value is outside the corresponding range.
  BEEn=0 The actual value is within the corresponding range.

To evaluate the RICH and BEE1 to 3 bits, transfer the position number with FREI=0, wait for the status bits, and then enable the IP outputs with FREI=1.

- Error bit ZBEV:
  ZBEV=1 The target range of the position (range BEE3) was exited without selection of a new position
- Reversal bit RIUM:
  RIUM=1 The BEE2 range was exited. This bit can be used to reverse the direction of travel when a position was ”overrun”.

When you configure the IP 240, you can allocate bits BEEn=0, ZBEV=1 and RIUM=1 to interrupt bits to trigger an interrupt, thus making it possible to control the auxiliary digital outputs via the interrupt service routine. Each interrupt is generated only once for a given position.

10.16 Reading and Evaluating the IP Status Information

This includes:
- the current (feedback) position number
- the status bits
- the current actual value
- the stored final value (is entered only in cyclic synchronization mode)

Table 10-20. Contents of the DB and the Transfer Buffer on Reading the Status Information

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 28	0	. . .		0	0	. . .		0	0	
DR 28	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	Feedback position number
DL 29	0	0	RIUM	ZBEV	UEBS	DRBR	NPUE	UEBL	2	Status bits
DR 29	DA2	DA1	MESE	BEE3	BEE2	BEE1	RICH	SYNC	3	
DL 30	SE								4	Actual value **in binary** A negative value is in two's complement representation. SE=Sign extension
DR 30	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	5	
DL 31	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	6	
DR 31	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	7	
DL **30**	SG				10^6				**4**	Actual value **in BCD** ”1111” is entered in the high-order nibble of DL30. (SG) for a negative number
DR **30**	10^5				10^4				**5**	
DL **31**	10^3				10^2				**6**	
DR **31**	10^1				10^0				**7**	
DL 32	SE								8	Final value **in binary** A negative value is in two's complement representation. SE=Sign extension
DR 32	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	9	
DL 33	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10	
DR 33	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	11	
DL **32**	SG				10^6				**8**	Final value **in binary** ”1111” is entered in the high-value nibble of DL32 (SG) for a negative number.
DR **32**	10^5				10^4				**9**	
DL **33**	10^3				10^2				**10**	
DR **33**	10^1				10^0				**11**	

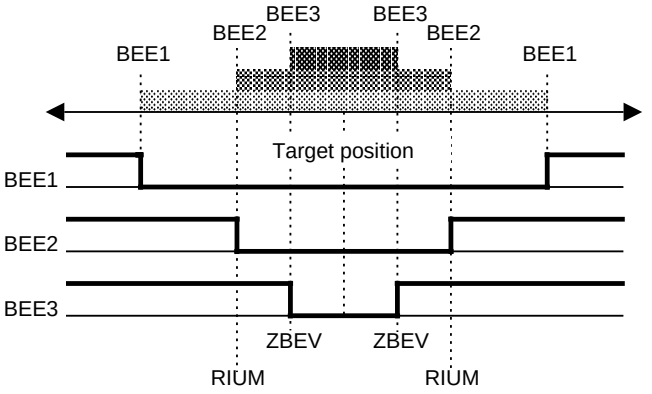
Reading the status information from the IP 240	
with control FB 168	**in direct data interchange**
You must initialize FB 168 as follows to read the status info: : JU FB 168 NAME : STEU.POS : FKT : 1,0	You must specify the following job numbers to read the status info: • For channel 1: $1B_H$ • For channel 2: $2B_H$
The FB reads the status info from the IP 240 and transfers it to DW 28 to 33 of the specified data block.	Following transfer of the job number, the IP 240 makes the status info available in the transfer buffer.

Evaluating the status information

Feedback position number
When a position is called, the position number is stored on the IP 240 as feedback position number. If synchronization bit SYNC is set, status bits BEE1, BEE2, BEE3, RICH, ZBEV and RIUM and their interrupt bits relate to this position number.
If you have not yet transferred a position number, or if the last position number was invalid, the IP 240 enters the value ”255”.
A position is invalid when
- an error occurred during actual value acquisition (DRBR, NPUE, UEBL).
- a reference point approach was selected or
- synchronization with an external control signal was selected via a one-shot transfer of ZYSY=1.

The status bits
The status bits are updated on the IP 240 in every firmware cycle.

Status bit	Bit is ”1”	Bit is ”0”
SYNC (synchronization)		The actual value is no longer synchronized
	The actual value is synchronized - via a reference point approach - via software-controlled synchronization - via an external control signal	Synchronization no longer available - when a reference point is reselected. - when resynchronization with an external control signal is initiated. - when an error occurs during actual value acquisition (DRBR, NPUE, UEBL).

<table>
<tr><th>Status bit</th><th>Bit is "1"</th><th>Bit is "0"</th></tr>
<tr><td rowspan="2">RICH
(direction)</td><td>Actual value not yet synchronized or no pos. no. active</td><td></td></tr>
<tr><td>- The target position must be approached from a negative direction (descending actual value).</td><td>- The target position must be approached from a positive direction (ascending actual value).
- The actual value indicates the target position.</td></tr>
<tr><td>BEE1
BEE2
BEE3</td><td colspan="2"> 
</td></tr>
<tr><td rowspan="2">Positioning
BEE1
BEE2
BEE3</td><td>Actual value not yet synchronized or no pos. no. active</td><td></td></tr>
<tr><td>Actual value outside relevant range.</td><td>Actual value at range limits or within relevant range.</td></tr>
<tr><td rowspan="2">Reference point approach (HASY=1)
BEE1</td><td>Preliminary contact not yet reached.

The preliminary contact was exited and BEE1=0 was read out from the IP 240 at least once.</td><td>Preliminary contact reached.</td></tr>
<tr><td>BEE2</td><td>Reference point not yet reached.

Reference point approach mode exited because HASY=0 transferred.</td><td>Reference point reached.</td></tr>
<tr><td rowspan="2">ZBEV
(target range exited)</td><td>Actual value exited range BEE3 without a new position number having been transferred.</td><td>New position number was transferred to IP 240.</td></tr>
<tr><td colspan="2">Note:
ZBEV is not set when the channel was configured with backlash compensation and range BEE2 is approached from a negative direction.</td></tr>
</table>

Status bit	Bit is "1"	Bit is "0"
RIUM (Reversal of direction)	Actual value exited range BEE2. Reversal of direction of travel is possible.	A new position number was transferred to the IP 240.
DA1 DA2 (IP output 1/2)	The relevant output is set.	Relevant output is reset.
DRBR (Wirebreak)	IP 240 detected wirebreak in symmetrical encoder.	Error was rectified and - the status info was read once with DRBR=1 or - the interrupt request bytes were read and the DRBR triggered the interrupt.
NPUE (Zero mark monitoring)	IP 240 detected zero mark error.	- The status info was read once with NPUE=1 or - the interrupt request bytes were read and NPUE triggered the interrupt.
UEBL (Overrange)	Actual value exited zero value range and entered the overrange.	- The status info was read once with UEBS=1 or - the interrupt request bytes were read and NPUE triggered the interrupt.
MESE UEBS (ZYSY=1)	The MESE and UEBS bits are relevant only when synchronization with an external control signal was selected	
MESE (Measuring terminated)	IP 240 detected a negative edge of the synchronization signal at the IN input and stored the current actual as final value.	- The final value was read.
UEBS (Final value overwritten)	Following a negative edge of the synchronization signal, the old final value was overwritten with the new final value without the old final value having been read.	- The status info was read once with UEBS=1 or - the interrupt request bytes were read and UEBS triggered the interrupt.

When they have been read, status bits NPUE, UEBL, MESE and UEBS are reset on the IP 240, i.e. these bits can be read out only once.

The actual value
The actual value is updated on the IP 240 in every firmware cycle.
Depending on how the channel was configured, the actual value is made available in either binary or BCD code.

The final value
The final value is updated only when synchronization with an external control signal was selected in parallel with actual value acquisition.
In this synchronization mode, the control signal at the IN input is used as synchronizing pulse:
- a positive edge of the IN signal initiates synchronization,
- a negative edge of the IN signal stored the current actual value as final value (of a count).

The final value is made available in either binary or BCD, depending on how the channel was configured.

10.17 Reading the Interrupt Request Bytes

During configuring, you specify which status bits are to trigger an interrupt. When an interrupt is generated (system interrupt or process interrupt), the S5 CPU invokes an interrupt service OB in which the IP 240's interrupt request bytes must be read. These bytes tell you which channel and which event triggered the interrupt.

When the interrupt request bytes are read,
- the bits in the interrupt request bytes on the IP 240 are reset,
- the interrupt request to the S5 CPU is revoked,
- status bit UEBL, DRBR, NPUE or UEBS is reset, depending on which triggered the interrupt.

Since the interrupt request bytes are read for both channels and the current state can be read out from the IP 240 only **once**, only the data block specified in control FB 168 can be immediately updated.

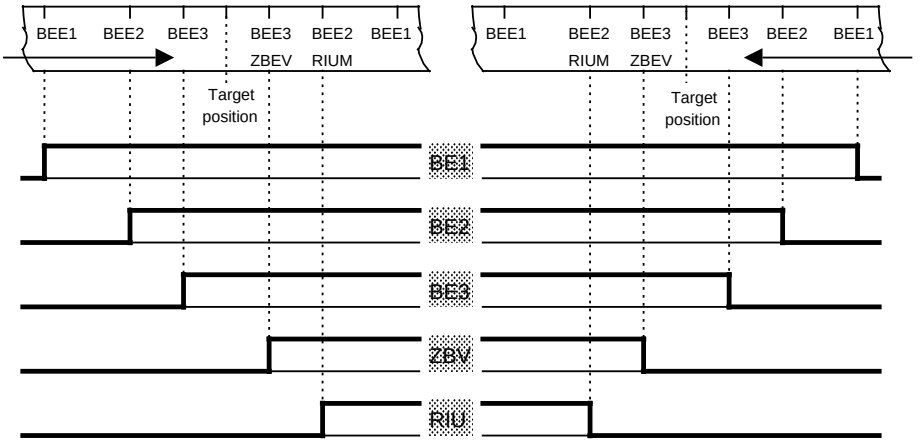
The interrupt request bytes shown in Table 10-21 are based on the assumption that both IP channels are being operated in positioning mode.

Reading the interrupt request bytes	
with control FB 168	**in direct data interchange**
You must initialize FB 168 as follows to read the interrupt request bytes: : JU FB 168 NAME : STEU.POS : FKT : 3,0 The FB reads the interrupt request bytes and transfers them to DW 20 to 21.	You must specify 31_H as job number for channels 1 and 2 to read the interrupt request bytes. Following transfer of the job number, the IP 240 makes the interrupt request bytes available in the transfer buffer.

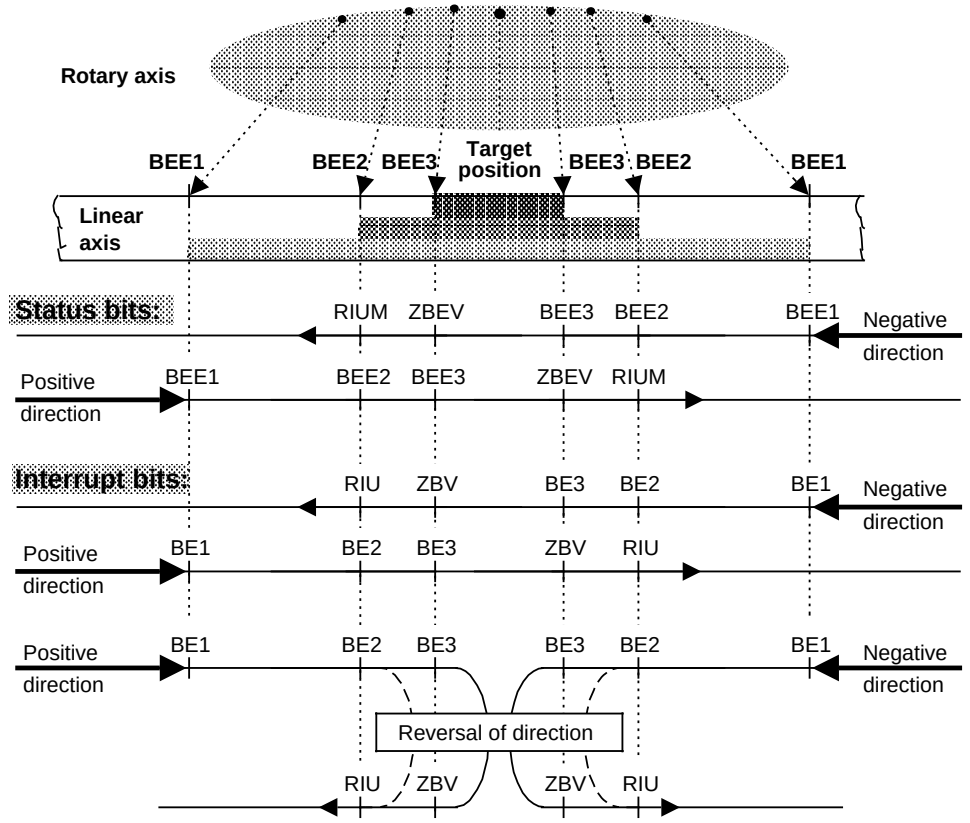
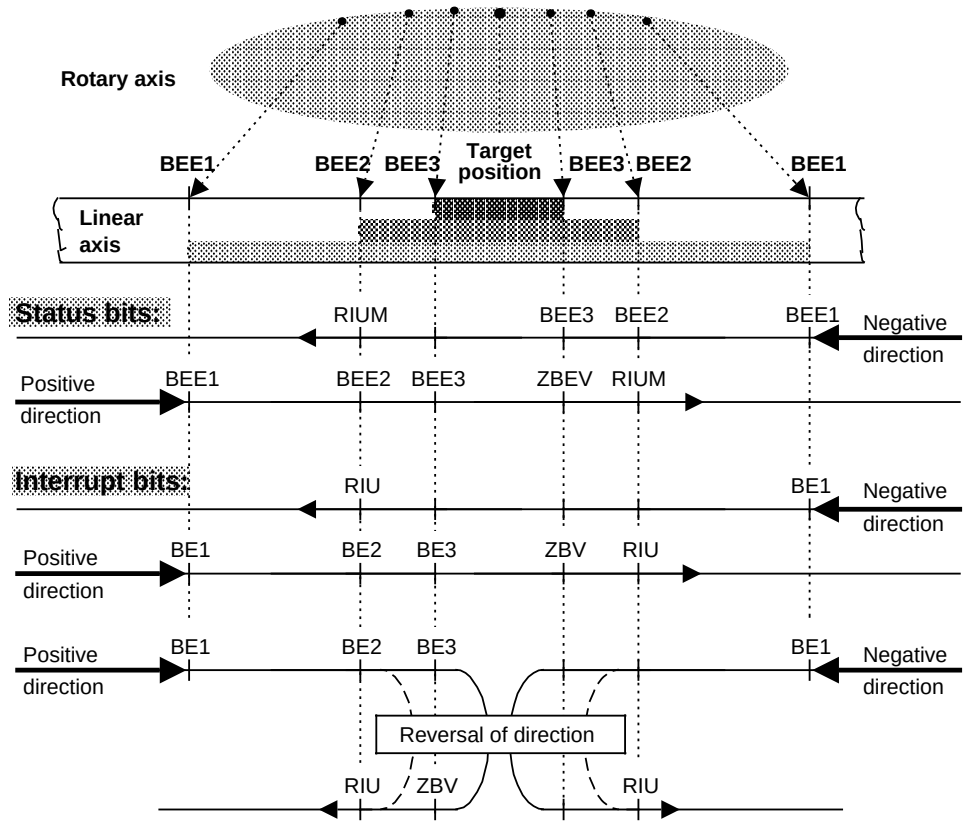
Table 10-21. Contents of the DB and the Transfer Buffer on Reading the Interrupt Request Bytes

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 20	0	0	RIU	ZBV	UBS	DRB	NPU	UEB	0	Interrupt request bytes for channel 1
DR 20	RICH	0	MES	BE3	BE2	BE1	0	0	1	
DL 21	0	0	RIU	ZBV	UBS	DRB	NPU	UEB	2	Interrupt request bytes for channel 2
DR 21	RICH	0	MES	BE3	BE2	BE1	0	0	3	

The bit that is ”1” shows the cause of the interrupt. When evaluating the interrupt request bytes, note that several bits may be ”1”.
Direction bit RICH has been included in the interrupt request bytes. This bit mirrors the current state of the RICH bit in the status area. It does not relate to the state of this bit when the interrupt occurred.

Interrupt bit	Bit is "1"
BE1 BE2 BE3	
Positioning BE1 BE2 BE3	Relevant range entered.
Reference point approach BE1	Preliminary contact reached.
Reference point approach BE2	Reference point reached.
ZBV (Target range exited)	The actual value has exited range BEE3 without a new position number having been selected.
RIU (Reversal of direction)	The actual value has exited range BEE2. A reversal of the direction of movement is possible.

Note:
If backlash compensation was configured, interrupts BE2, BE3 and ZBV are generated during positioning only when range BEE2 was entered from a positive direction.

	Examples for interrupt bits BE1 to BE3, ZBV and RIU
Without backlash compensation	
With backlash compensation	

Interrupt bit	Bit is "1"
DRB (Wirebreak)	The IP 240 detected a wirebreak in a symmetrical encoder.
NPU (Zero mark monitoring)	The IP 240 detected a zero mark error.
UEB (Overflow)	The actual value has exited the valid actual value range and entered the overrange.
MES UBS	The MES and UBS bits are relevant only when synchronization with an external control signal was selected in parallel with actual value acquisition.
MES (Measuring terminated)	The IP 240 detected a negative edge of the synchronization signal at the IN input and stored the current actual value as final value.
UBS (Over-written)	Following a negative edge of the synchronization signal, the old final value was overwritten with the new final value without the old final value having been read.

10.18 Modifying the Position Data and the Zero Offset

The position values, the distance values of the switching and signalling ranges and the zero offset are transferred to the IP 240 for the first time during configuring. After configuring, you can modify these data. The position numbers are defined during the configuring phase only; they cannot be subsequently modified, nor can new position numbers be defined.
To prevent data interchange from unduly increasing the channel's response time, you can transfer new position values only when the IP outputs are disabled. Over the STEP 5 program, you must ensure that the increase in the cycle time does not excessively on-load the other IP channel. You can check the state of the IP outputs by reading status bits DA1 and DA2. If it is necessary to disable the outputs, you can do so by transferring control bit FREI=0.

The following ranges of values are permissible for new data:

Range of values for	Range limits	Number format	
		Binary	BCD
The position value for a linear axis	-9,999,999 to+9,999,999	•	•
The position value for a rotary axis	0 to [final value for rotary axis - 1]	•	•
The distance values for ranges BEE1, BEE2 and BEE3 (additional values for a rotary axis)	0 to 999,999 (but not exceeding 0.5·[final value for rotary axis])	•	•
Zero offset (additional values for a rotary axis)	-9,999,999 to+9,999,999 (but not exceeding [final value for rotary axis])	•	•

Note the following when choosing the distance values:
Distance for range BEE1 distance for BEE2 distance for BEE3

The modified data go into force as soon as they are transferred. The IP 240 updates the status bits and generates any pending interrupts. However, the IP outputs are not set. To set the outputs, you must retransfer the position number.

10.18.1 Modifying the Position Value

When you want to change a position value for position 1 to 254, you must specify the new position value and the associated position number. You can modify two position values per data interchange. If you transfer ”255” as position number, the associated position value is not evaluated.

Table 10-22. Contents of the Data Block and the Transfer Buffer for Modifying Position Values

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL n	0	. . .		0	0	. . .		0	0	
DR n	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	1st position number
DL n+1	SE								2	1st position value **in binary**
DR n+1	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	3	A negative value must be represented as two's complement. SE=Sign extension
DL n+2	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	4	
DR n+2	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	5	
DL **n+1**	SG			10^6					**2**	1st position value **in BCD**
DR **n+1**	10^5			10^4					**3**	”1111” must be entered in the high-order nibble of DL n+1 (SG) for a negative number.
DL **n+2**	10^3			10^2					**4**	
DR **n+2**	10^1			10^0					**5**	
DL n+3	0	. . .		0	0	. . .		0	6	
DR n+3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	7	2nd position number
DL n+4	SE								8	2nd position value **in binary**
DR n+4	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	9	A negative value must be represented as two's complement. SE=Sign extension
DL n+5	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10	
DR n+5	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	11	
DL **n+4**	SG			10^6					**8**	2nd position value **in BCD**
DR **n+4**	10^5			10^4					**9**	”1111” must be entered in the high-order nibble of DL n+4 (SG) for a negative number.
DL **n+5**	10^3			10^2					**10**	
DR **n+5**	10^1			10^0					**11**	

n= 57+3 • (number of the entry)

If you use FB 168 to write the new position values, you must specify the entry to be transferred in the data block when you initialize the FKT parameter. Based on this information, the FB checks the length of the DB and computes the number of data words to be transferred. You can also specify whether you want to transfer only one entry or two continuous DB entries to the IP 240.
The position numbers and position values reserve the data words from DW 60 in the data block.

Transferring new position values for positions 1 to 254	
with control DB 168	**in direct data interchange**
You must first update the position values in the DB. Using FB 168, you can then transfer either one or two position entries to the IP 240. You must initialize the FB as follows: : JU FB 168 NAME : STEU.POS : FKT : 41,y y=Number of the **entry** to be transferred; must be a number between 1 and 255 FKT : 42,y y=Number of the first of the two **entries** to be transferred; must be a number between 1 and 255	You must specify the following job numbers to transfer the new position values: • For channel 1: 11_H • For channel 2: 21_H If you want to change only one position value, you must specify ”255” for the second position number.
Note that the number of the **entry** in the data block, **not the position number**, must be specified when you call the FB.	If the bytes with offset 0 and 6 are also to be transferred, they must first be set to ”0”.

Example:
Modified position values for entries 8 and 9 are to be transferred to the IP 240. The data block containing these data is DB12. Errors are to be flagged in flag byte FY 12.

```
      :  JU FB 168
NAME  :  STEU.POS
DBNR. :  KF + 12
FKT   :  KY 42,8
                 |  |
                 |  |_____=Transfer the data beginning with entry 8
                 |
                 |________= Transfer two entries
PAFE  :  FY 12
```

If you transfer two position values and one of them is errored, only the errored data is rejected.

Positions in excess of 65 require a DB comprising more than 256 words. Data words with a data word number greater than 255 can be addressed only with the supplementary STEP 5 commands (system operations) (Section 10.24).

10.18.2 Changing the Distance Values for Ranges BEE1 to BEE3

Table 10-23. Contents of the Data Block and the Transfer Buffer for Changing Distance Values

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 50	0	. . .		0	0	. . .		0	0	Distance value for range BEE1 **Binary**
DR 50	0	. . .		0	2^{19}	2^{18}	2^{17}	2^{16}	1	
DL 51	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2	
DR 51	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	3	
DL **50**	0				0				**0**	Distance value for range BEE1 **BCD**
DR **50**	10^{5}				10^{4}				**1**	
DL **51**	10^{3}				10^{2}				**2**	
DR **51**	10^{1}				10^{0}				**3**	
DL 52	0	. . .		0	0	. . .		0	4	Distance value for range BEE2 **Binary**
DR 52	0	. . .		0	2^{19}	2^{18}	2^{17}	2^{16}	5	
DL 53	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	6	
DR 53	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	7	
DL **52**	0				0				**4**	Distance value for range BEE2 **BCD**
DR **52**	10^{5}				10^{4}				**5**	
DL **53**	10^{3}				10^{2}				**6**	
DR **53**	10^{1}				10^{0}				**7**	
DL 54	0	. . .		0	0	. . .		0	8	Distance value for range BEE3 **Binary**
DR 54	0	. . .		0	2^{19}	2^{18}	2^{17}	2^{16}	9	
DL 55	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	10	
DR 55	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	11	
DL **54**	0				0				**8**	Distance value for range BEE3 **BCD**
DR **54**	10^{5}				10^{4}				**9**	
DL **55**	10^{3}				10^{2}				**10**	
DR **55**	10^{1}				10^{0}				**11**	

Transferring modified distance values for the switching and signalling ranges	
with control FB 168	**in direct data interchange**
You must first enter the new distance values in the data block. Initialize the FB as follows: : JU FB 168 NAME : STEU.POS : FKT : 6,0	You must specify the following job numbers to transfer the new distance values: • For channel 1: 10_H • For channel 2: 20_H If the bytes with offset 0, 4 and 8 are also transferred, they must first be set to ”0”.

10.18.3 Changing the Zero Offset

You can specify either a relative or an additive zero offset (NVER).
The actual value is modified as follows when a zero offset is transferred:

Relative zero offset

$$Actual_{\mathbf{new}} = Actual_{\mathbf{old}} + Zero\ offset_{\mathbf{rel.,\ new}} - Zero\ offset_{\mathbf{rel.,\ old}}$$

Additive zero offset

$$Actual_{\mathbf{new}} = Actual_{\mathbf{old}} + Zero\ offset_{\mathbf{add.,\ new}}$$

You can transfer relative or additive zero offsets in any order. Note, however, that the next relative zero offset to follow an additive zero offset is based on the value $NVER_{\mathbf{rel.,old}}=0$.

Example: Actual value=0

NVER = 1000 is specified as **relative** zero offset:
Actual value=1000

NVER = 500 is specified as **additive** zero offset:
Actual value=1500

NVER = 2000 is specified as **relative** zero offset:
Actual value=3500

NVER = 1500 is specified as **relative** zero offset:
Actual value=3000

Every time the actual value is synchronized, it is set to the value of the zero offset last transferred, regardless of whether this was a relative or an additive zero offset.

In direct data interchange, the ADD bit is used to specify the type of zero offset:
ADD=0 for a relative zero offset
ADD=1 for an additive zero offset

Table 10-24. Contents of the Data Block and the Transfer Buffer for Changing the Zero Offset

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 45	0	. . .		0	0	. . .		0	0	
DR 45	0	0	0	0	0	0	0	ADD	1	Control bit ADD
DL 46	SE								2	Zero offset **in binary**
DR 46	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	3	
DL 47	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	4	A negative value must be given as two's complement. SE=Sign extension
DR 47	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	5	
DL **46**	SG				10^{6}				**2**	Zero offset **in BCD**
DR **46**	10^{5}				10^{4}				**3**	
DL **47**	10^{3}				10^{2}				**4**	”1111” must be entered in the high-order nibble of DL 46 (SG) for a negative number.
DR **47**	10^{1}				10^{0}				**5**	

Transferring a zero offset	
with control FB 168	**in direct data interchange**
The new zero offset value must be entered in DW 46 to 47. The type of zero offset is specified when you initialize the FB. Initialize the FB as follows: : JU FB 168 NAME : STEU.POS : FKT : 5,y y=0 Relative zero offset y >0 Additive zero offset The function block transfers the relevant identifier to data word 45.	You must specify the following job numbers to transfer a new zero offset: • For channel 1: 19_H • For channel 2: 29_H Select the type of zero offset via bit 0 of offset 1. The byte with offset 0 must be set to ”0”.

10.19 Interrupting Positioning and Skipping of a Position

Positioning is interrupted when

- control bit FREI=0 is transferred.
  In this case, the outputs are disabled but the old position number is retained. If the actual value changes (e.g. due to transfer of a zero offset), the status bits are matched to this position number and any pending interrupts generated in dependence on the actual value.
  You can enable the outputs by transferring FREI=1. The position number must be reselected.

- an error occurs during signal acquisition (overrange, wirebreak/short-circuit in a symmetrical encoder or a zero mark error).
  When an error occurs,
  - the IP outputs are immediately disabled when they are under the control of the IP 240 module firmware (HAND=0),
  - the old position is invalidated and ”255” entered as feedback position number and
  - the SYNC bit is set to ”0”.

Skipping of a position
If a position is ”skipped” because of excessively fast changes in the actual value, all interrupts still pending for this position are generated and the outputs are disabled (LOSE=0).

10.20 Start of Positioning within a BEE Range

If the actual value is already within a BEE range when a position is selected, the associated interrupts are generated immediately.

Actual value is in range BEE3 (target range)
If you structured the IP 240 for backlash compensation, note the following:
In order to ensure that each position is always approached from the same direction, the target range must first be exited. To do this, you can either specify another position with a lower position number or you can control the IP outputs over the S5 CPU.
The following steps are required to exit the target range via output control:
- By controlling the outputs via the S5 CPU, the target range must be exited in a negative direction. To do this, you must initialize control bits DA1S and DA2S in accordance with the DAV parameter, and transfer them together with HAND=1 and FREI=1.
- When status bit RIUM or interrupt bit RIU is ”1”, the BEE2 range has been exited.
- The IP outputs must be disabled via the S5 CPU.
- Reselect the position and enable the IP outputs.

Actual value is in range BEE2
If the actual value is within range BEE2 and outside the target range when the target position is selected, the target range must be approached by controlling the IP outputs via the S5 CPU or the drive must be moved out of range BEE2 and positioning repeated. This requires the same steps as those needed to exit the target range.

If the channel was structured for backlash compensation and the actual position is above the target position (RICH=1), output D2 is automatically set if the IP outputs have been enabled. When the BEE2 range is exited, the IP output must be reset via the S5 CPU by transferring control bit FREI=0 to the IP 240.

The following table shows you how the IP 240 uses the various combinations of status bits BEE1 to BEE3 to set the IP outputs and generate interrupts. Note the differences produced by backlash compensation/no backlash compensation.

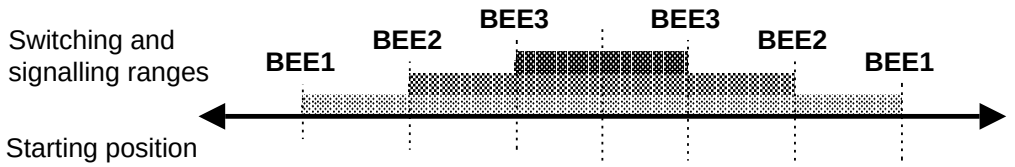


Table 10-25. IP Responses at the Start of Positioning

States of the status bits following selection of the new target position				Without backlash compensation								
				Outputs set DAV =0		DAV=1		DAV=2		Interrupts generated		
BEE1	BEE2	BEE3	RICH	D1	D2	D1	D2	D1	D2	BE1	BE2	BE3
1	1	1	0	X		X	X	X				
0	1	1	0		X		X	X		X		
0	0	1	0							X	X	
0	0	0	0							X	X	X
0	0	0	1							X	X	X
0	0	1	1							X	X	
0	1	1	1		X		X		X	X		
1	1	1	1	X		X	X		X			

States of the status bits following selection of the new target position				With backlash compensation								
				Outputs set DAV =0		DAV=1		DAV=2		Interrupts generated		
BEE1	BEE2	BEE3	RICH	D1	D2	D1	D2	D1	D2	BE1	BE2	BE3
1	1	1	0	X		X	X	X				
0	1	1	0		X		X	X		X		
0	0	1	0							X	X	
0	0	0	0							X	X	X
0	0	0	1							X	X	X
0	0	1	1		X		X		X	X		
0	1	1	1		X		X		X	X		
1	1	1	1	X		X	X		X			

X=Output is set or an interrupt generated and the corresponding interrupt bits are set

E.g.: Start in zone	BEE2=0/BEE3=1	The drive is between cut-off point and target range.
	RICH=1	The drive is above the target position.
	Interrupt BE1	The drive must traverse at creep speed .
	DA2=1	The drive switched on to ”overrun the position” via D2.

10.21 Positioning with the IP 240

The flowchart below illustrates the functional sequence for positioning with the IP 240.
In the examples, no checks are made for errors such as skipping of a position or wirebreak.

10.21.1 Positioning with the IP Controlling the Speed

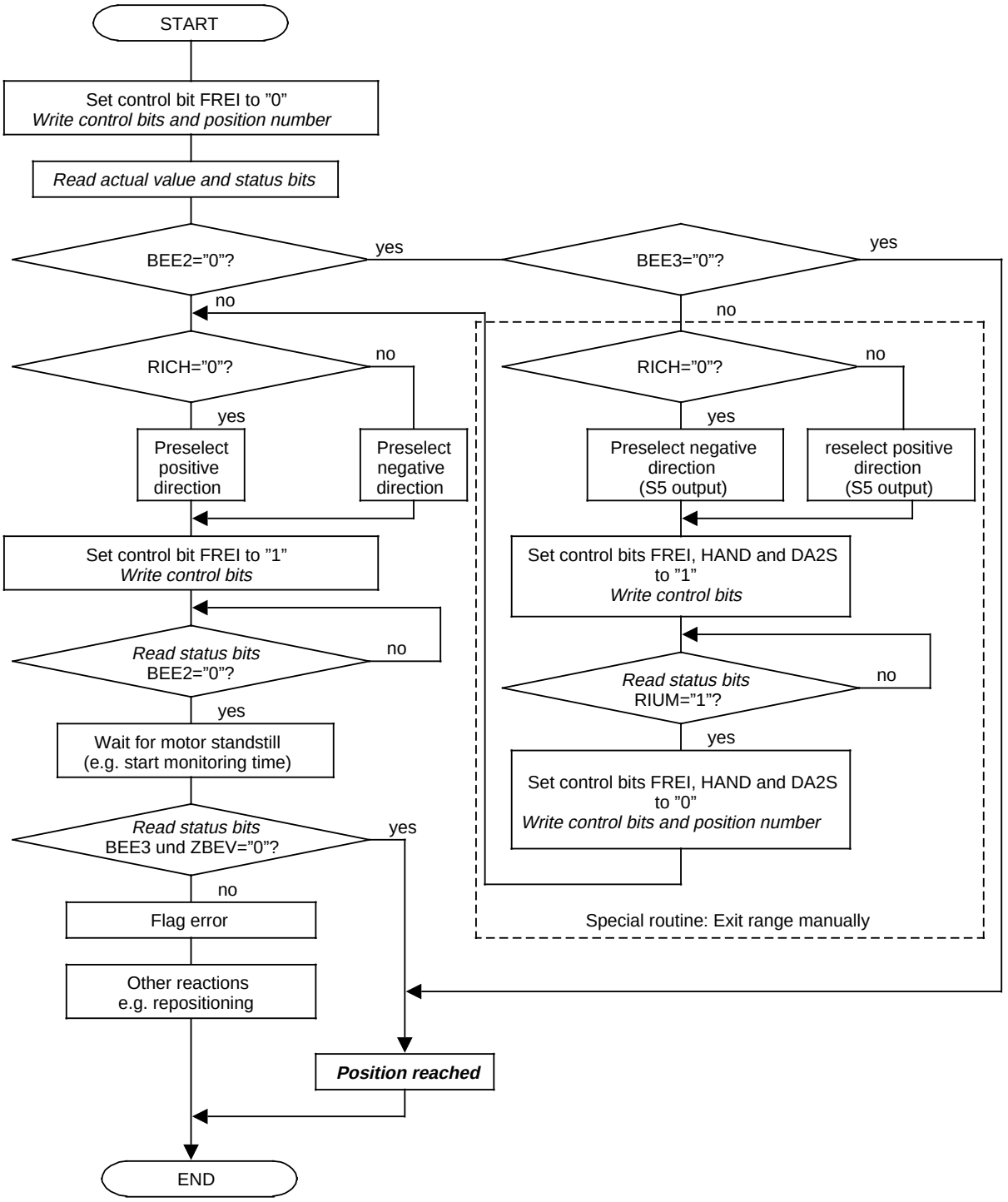


Fig. 10-31. Positioning with the IP 240 Controlling the Speed, without Backlash Compensation, Axis with Two Speeds and Two Directions of Travel

10.21.2 Positioning with the IP Controlling the Direction

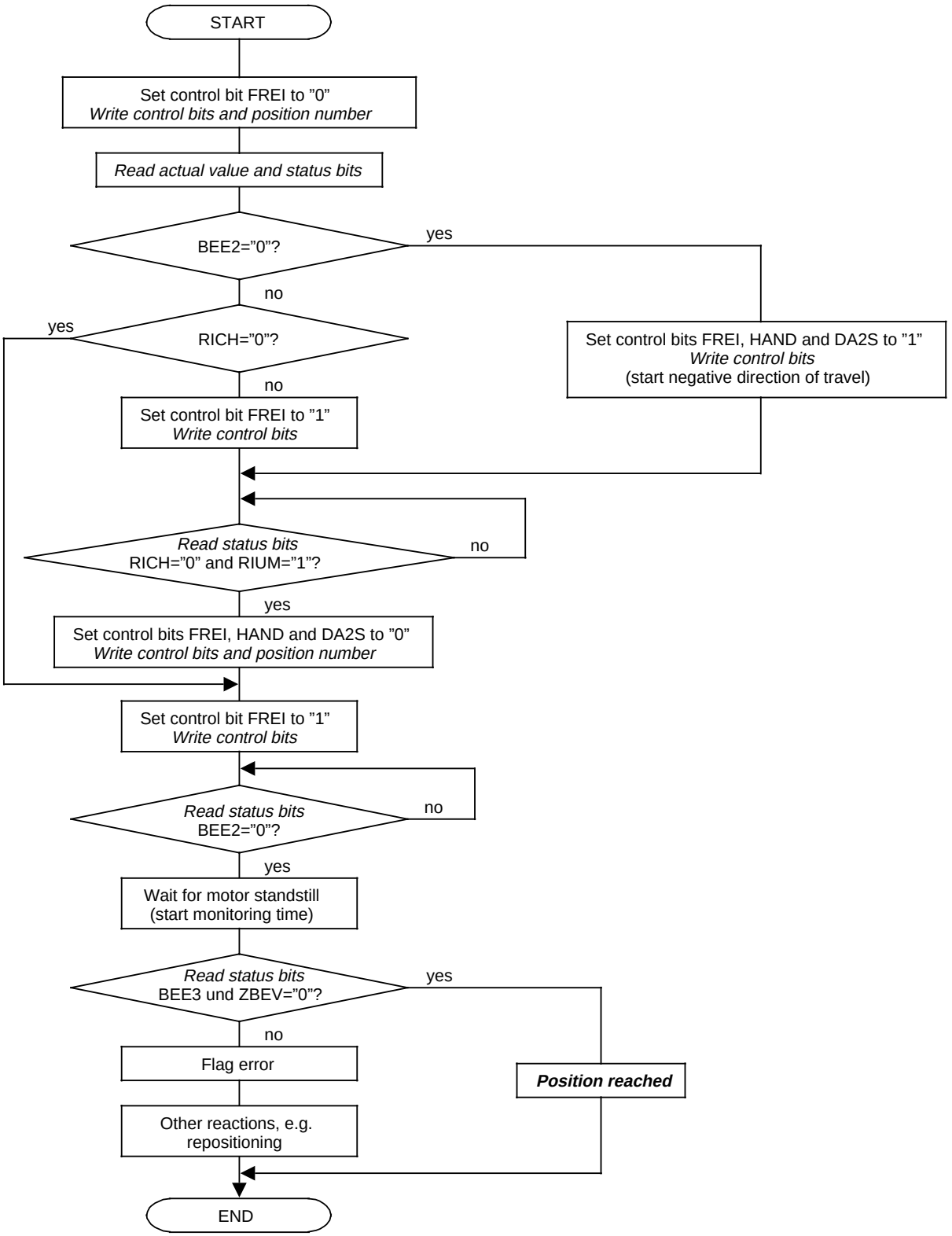


Fig. 10-32. Positioning with the IP 240 Controlling the Direction of Travel, with Backlash Compensation, without Rotary Axis, Axis with One Speed and Two Directions of Travel

10.22 Error Processing Following Positioning Control

Errors occurring during transfer of data to the IP are flagged
- in the PAFE byte when FB 168 is used and
- in the IP's status register when using direct data interchange (Chapter 11).

Warning

The PAFE byte or IP 240 status register must be evaluated after every data interchange. In the event of an error, it may be necessary to interrupt positioning instantaneously by disabling the outputs.

Errors in FB parameters are detected by the FB and described in more detail in DW13 of the specified data block. The FBs must be reinvoked after correcting the relevant parameters.
The data transferred is checked by the IP 240 module firmware. If an error is detected,
- the incorrect values are rejected. The only exception is control bit FREI=0. The channel's outputs are also disabled if an illegal control bit combination or invalid position number is detected.
- a detailed description of the error is entered in the ”error flag” area on the IP.

Reading the error flags from the IP 240	
with control FB 168	**in direct data interchange**
FB 168 reads the error flags automatically when an error is detected. The data is transferred to DW 8 to 10.	You must specify job number 01_H to read the error flags. The IP then makes these flags available in the transfer buffer.

Table 10-26. Contents of the Data Block and the Transfer Buffer on Reading Error Flags

Data byte in data block	Bit 7	6	5	4	3	2	1	0	Offset in transfer buffer	Description
DL 8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	Error no. 3
DR 8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	1	Extension to error no. 3
DL 9	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2	Error no. 2
DR 9	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	3	Extension to error no. 2
DL 10	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4	Error no. 1
DR 10	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	5	Extension to error no. 1

The error number and the error extension are in KH format.
When the transfer buffer has been read out, the error flags are reset on the IP 240. They must be reset in the DB via the STEP 5 program.
You will find a complete list of error codes in Chapter 14.

10.23 Data Block Contents and Initializing the Standard Function Blocks

10.23.1 The Data Block

Creating the data block

The standard function blocks (configuring FB and control FB) use a data block (DB) to interchange data with the IP 240. You must create this data block and enter the required data prior to the first FB call.

The length of the data block depends on the number of positions you want to store. The minimum length is 60 data words (data word 0 to data word 59), and increases by 3 words for each position. If, for instance, 65 positions are entered, the data block must comprise 60+3·65=255 data words (data word 0 to data word 254). For 254 positions, the data block would have to comprise 822 data words.

When the configuring FB is invoked, the length of the DB is checked on the basis of the number of positions to be transferred, which is in DR 58. When the control FB is invoked to change the position data, the length of the DB is checked on the basis of the entry number specified in the FKT parameter. If there is a discrepancy, the FB sets bit 2 in the PAFE byte.

Note that data words from DW 256 on can be addressed only with supplementary STEP 5 commands (system operations), e.g. ”LIR” and ”TIR” (Section 10.24).

In the S5-135U and S5-155U, you can also create the data block in the extended DB area (DX area).

Specifying the data block number

The data block number is specified in the DBNR parameter.

During configuring, you must specify the number of the data block created. FB 167 opens this data block.

After configuring you can either

- use a DB that is already opened. In the S5 115U, this function is only available from CPU 943 onwards.
- or specify the DB number, so that the DB is opened by FB 168.

The FB is to open the data block you created:

S5-115U and S5-150U				S5-135U and S5-155U			
	: JU FB167		: JU FB 168		: JU FB 168		: JU FB 168
NAME	: STRU.POS	NAME	: STEU.POS	NAME	: STRU.POS	NAME	: STEU.POS
	:		:		:		:
DBNR	: KF y	DBNR	: KF y	DBNR	: KY x,y	DBNR	: KY x,y

y=3 to 255	Number of the data blockcreated
x=0	DB created in normal DB area
x=1	DB created in extended DB area

The data block that was already opened is to be used:

S5-115U and S5-150U				S5-135U and S5-155U			
			: JU FB 168				: JU FB 168
		NAME	: STEU.POS			NAME	: STEU.POS
			:				:
		DBNR	: KF y			DBNR	: KY x,y

y=0	the data block that was already opened is to be used
x=0	Regardless of whether the DB was created in the normal or in the extended DB area

Contents of the data block

Table 10-27. Contents of the Data Block (DW 0 to DW 821)

DW 0	
DW 1 to 3	**Machine-readable product designation of the module**
DW 4 to 6	**Module firmware version**
DW 7	**Module hardware version**
DW 8 DW 9 DW 10	**Error flags for hardware, communications and data errors**
DW 11 to 12	
DW 13	**Error flags for parameter assignment errors**
DW 14 to 18	
DW 19	**Function number for indirect initialization of the control FB**
DW 20 DW 21	**Interrupt request bytes for channel 1** **Interrupt request bytes for channel 2**
DW 22	
DW 23	**ID for the configured mode and DB no.**
DW 24 to 25	
DW 26 to 27	**Absolute address of the configured module**
DW 28	**Feedback position number**
DW 29	**Status bits**
DW 30 to 31	**Actual value**
DW 32 to 33	**Final value**
DW 34	
DW 35 DW 36	**Control bits and position number for pos. 1 to 254**
DW 37 to 44	**Data for position 0** **- Position value** **- Distance values for BEE1 to BEE3 for position 0**
DW 45 to 47	**Zero offset**
DW 48 to 49	**Final position of the rotary axis**
DW 50 to 55	**Distance values for BEE1 to 3 for positions 1 to 254**
DW 56 to 57	
DW 58	**Number of positions to be transferred**
DW 59	
DW 60 DW 61 DW 62	**Position number** **Position value (1st entry)**
DW 63 DW 64 DW 65	**Position number** **Position value (2nd entry)**
DW 66 to 255	**Position data for entries 3 to 65**
DW 256 to 821	**Position data for entries 66 to 254**

This data can be forwarded from the DB to the IP 240, and must first be updated in the DB.

If you want to read the actual values in these data areas, you must first invoke the control FB and initialize it for Read function 1,0 or 3,0.

This data is specified when the configuring FB is initialized or transferred from the IP 240 to the DB when the module is configured.

These data words are used internally, and may not be modified.

This data word is unassigned, and you can use it as you see fit.

Contents of the data words
You must set the unassigned positions of the data words you want to transfer to the IP 240 to ”0”.

Function number for indirect initialization of control FB 168

Data byte	Bit 7	6	5	4	3	2	1	0	FKT: KY x,y
DL 19	0	0	2^5	2^4	2^3	2^2	2^1	2^0	FKT x
DR 19	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	FKT y

You can enter the FKT number for indirect initialization of the control function block in these two bytes.

Interrupt request bytes for channel 1 and channel 2

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 20	0	0	RIU	ZBV	UBS	DRB	NPU	UEB	Channel 1
DR 20	RICH	0	MES	BE3	BE2	BE1	0	0	Channel 1
DL 21	0	0	RIU	ZBV	UBS	DRB	NPU	UEB	Channel 2
DR 21	RICH	0	MES	BE3	BE2	BE1	0	0	Channel 2

RIU = 1 The interrupt was triggered because range BEE2 was exited (reversal of direction possible)

ZBV = 1 The interrupt was triggered because the target range was exited.

UBS = 1 The interrupt was triggered because the final value (final position) was overwritten.

DRB = 1 The interrupt was triggered because of a wirebreak/short-circuit.

NPU = 1 The interrupt was triggered because of a zero mark error.

UEB = 1 The interrupt was triggered because the count entered the overrange

RICH = 1 The actual value must be modified in negative direction (descending actual value) in order to reach the target position.

RICH = 0 The actual value must be modified in positive direction (ascending actual value) in order to reach the target position.
The bit is taken from the status area, and does **not** trigger an interrupt.

MES = 1 The interrupt was triggered when the final position was stored.

BE3 = 1 The interrupt was triggered on entering range BEE3.

BE2 = 1 The interrupt was triggered on entering range BEE2 or on reaching the reference point.

BE1 = 1 The interrupt was triggered on entering range BEE1 or on reaching the preliminary contact.

ID for the configured mode and data block number

Data byte	Bit 7	6	5	4	3	2	1	0	
DL 23	0	0	0	0	0	1	0	0	
DR 23	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DB no.

Following error-free configuring of the channel, a bit combination identifying the current mode is entered in DL 23.

DL 23 = 04_H The channel was configured for ”positioning” mode.

DR 23 = Number of the data block (in binary)

Absolute address of the configured module

Data byte	Bit 7	6	5	4	3	2	1	0
DL 26	0	0	0	0	0	0	0	0
DR 26	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}
DL 27	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
DR 27	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The configuring FB enters the absolute start address of the configured module in these bytes. You can use this address for programming direct data interchange with the IP 240.

Feedback position number

Data byte	Bit 7	6	5	4	3	2	1	0
DL 28	0	0	0	0	0	0	0	0
DR 28	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The bits in the status area refer to this position number.
If no position has been selected, the IP 240 returns number ”255”.

Status bits

Data byte	Bit 7	6	5	4	3	2	1	0
DL 29 DR 29	0 DA2	0 DA1	RIUM MESE	ZBEV BEE3	UEBS BEE2	DRBR BEE1	NPUE RICH	UEBL SYNC

RIUM = 1 Range BEE2 was exited (reversal of direction possible).

ZBEV = 1 The target range (BEE3) was exited.

UEBS = 1 The stored final position was overwritten without being read out from the IP 240.

DRBR = 1 Wirebreak/short-circuit in symmetrical encoder.

NPUE = 1 Zero mark error.

UEBL = 1 Overrange.

DA2 = 1 Digital output D2 is set.
= 0 Digital output D2 is not set.

DA1 = 1 Digital output D1 is set.
= 0 Digital output D1 is not set.

MESE = 1 The current actual position was stored as final position.

BEE 3 = 1 The actual value is outside range BEE3.
= 0 Range BEE3 entered.

BEE 2 = 1 The actual value is outside range BEE2.
= 0 Range BEE2 entered.

BEE 1 = 1 The actual value is outside range BEE1.
= 0 Range BEE1 entered.

RICH = 1 The actual value must be modified in negative direction (descending value) in order to reach the target position.
= 0 The actual value must be modified in positive direction (ascending value) in order to reach the target position.

SYNC = 1 The actual value (i.e. actual position) is synchronized.

Actual value

	Binary representation								BCD representation							
Data byte	Bit 7	6	5	4	3	2	1	0	Bit 7	6	5	4	3	2	1	0
DL 30 DR 30 DL 31 DR 31	SE 2^{23} 2^{15} 2^{7}	SE 2^{22} 2^{14} 2^{6}	SE 2^{21} 2^{13} 2^{5}	SE 2^{20} 2^{12} 2^{4}	SE 2^{19} 2^{11} 2^{3}	SE 2^{18} 2^{10} 2^{2}	SE 2^{17} 2^{9} 2^{1}	SE 2^{16} 2^{8} 2^{0}	SG 10^{5} 10^{3} 10^{1}				10^{6} 10^{4} 10^{2} 10^{0}			
	Negative values are represented as two's complement SE=Sign extension								The high-order nibble (SG) is ”1111” when the value is negative							

Final value

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 32 DR 32 DL 33 DR 33	SE 2^{23} 2^{15} 2^{7}	SE 2^{22} 2^{14} 2^{6}	SE 2^{21} 2^{13} 2^{5}	SE 2^{20} 2^{12} 2^{4}	SE 2^{20} 2^{12} 2^{4}	SE 2^{18} 2^{10} 2^{2}	SE 2^{17} 2^{9} 2^{1}	SE 2^{16} 2^{8} 2^{0}	SG 10^{5} 10^{3} 10^{1}				10^{6} 10^{4} 10^{2} 10^{0}			
	Negative values are represented as two's complement. SE=Signal extension								The high-order nibble (SG) is ”1111” for a negative number.							

Control bits and position number for position 1 to 254

Data byte	**Bit**								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
DL 35	0	0	0	0	0	0	0	0	
DR 35	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Position no.
DL 36	AMSK	ZYSY	SOSY	HASY	DA2S	DA1S	HAND	FREI	Control bits
DR 36	0	0	0	0	0	0	0	0	

Position number:
The new position number is entered in DR 35.
Permissible range of values: 1 to 254
When the standard FBs are used, the FB enters the position number.

Control bits:

AMSK = 1 All interrupts for the channel are masked, i.e. lost.
= 0 Interrupts enabled.

ZYSY = 1 Enable for synchronization with an external control signal.

SOSY = 1 Enable for software-controlled synchronization.

HASY = 1 Enable for synchronization via reference point approach.

DA2S = 1 Digital output 2 is to be set when HAND=1 and FREI=1. *)

= 0 Digital output 2 is to be reset when HAND=1 and FREI=1.

DA1S = 1 Digital output 1 is to be set when HAND=1 and FREI=1.*)

= 0 Digital output 1 is to be reset when HAND=1 and FREI=1.

HAND = 1 The state of the outputs is determined by DA1 and DA2 *)
= 0 The state of the outputs is controlled by the module firmware on the basis of the actual value.

FREI = 1 The IP outputs are enabled.
= 0 The IP outputs are disabled.

*) When DAV=2, the direction for a reference point approach must be specified via DA1S=1 or DA2S=1 with HAND=0.

Data for position 0

Position value for position 0

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 37 DR 37 DL 38 DR 38	SE 2^{23} 2^{15} 2^{7}	SE 2^{22} 2^{14} 2^{6}	SE 2^{21} 2^{13} 2^{5}	SE 2^{20} 2^{12} 2^{4}	SE 2^{19} 2^{11} 2^{3}	SE 2^{18} 2^{10} 2^{2}	SE 2^{17} 2^{9} 2^{1}	SE 2^{16} 2^{8} 2^{0}	SG 10^{5} 10^{3} 10^{1}				10^{6} 10^{4} 10^{2} 10^{0}			
	Negative values are represented as two's complement. SE=Sign extension								”1111” must be entered in the high-order nibble (SG) for a negative number.							

Permissible values:
- From - 9,999,999 to+9,999,999 for a linear axis
- From 0 to+[final pos. of linear axis - 1] for a rotary axis

Distance values for ranges BEE1 to 3 for position 0

Distance value for range BEE1

Data byte	**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL39	0	0	0	0	0	0	0	0
DR39	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}
DL40	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
DR40	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Distance value for range BEE2

Data byte	**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL41	0	0	0	0	0	0	0	0
DR41	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}
DL42	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
DR42	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Permissible values:
- From 0 to 999,999 for a linear axis
- From 0 to 0.5·[final pos. of rotary axis], but not exceeding 999,999 for a rotary axis

Note the following when choosing the distance values:
Distance for range BEE1 distance for range BEE2 distance for BEE3

Distance value for range BEE3

Data byte	Bit 7	6	5	4	3	2	1	0
DL43	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
DR43	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Control bit for the distance values

Data byte	Bit 7	6	5	4	3	2	1	0
DL44	0	0	0	0	0	0	0	GAUE
DR44	0	0	0	0	0	0	0	0

GAUE = 1 Use specified distance values.
= 0 Use distance values stored on the IP.

Zero offset
Control bit for the zero offset

Data byte	Bit 7	6	5	4	3	2	1	0
DR 45	0	0	0	0	0	0	0	ADD

ADD = 1 Additive zero offset
= 0 Relative zero offset

Zero offset value

	Binary representation								BCD representation							
Data byte	Bit 7	6	5	4	3	2	1	0	Bit 7	6	5	4	3	2	1	0
DL 46	SE	SE	SE	SE	SE	SE	SE	SE	SG				10^{6}			
DR 46	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^{5}				10^{4}			
DL 47	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	10^{3}				10^{2}			
DR 47	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	10^{1}				10^{0}			
	Negative values must be represented as two's complement. SE=Signal extension								”1111” must be entered in the high-order nibble (SG) for a negative number.							

Permissible values:
- From - 9,999,999 to+9,999,999 for a linear axis
- From 0 to±[final pos. of the rotary axis] for a rotary axis

Final position of the rotary axis

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 48	0	0	0	0	0	0	0	0	0				10^6			
DR 48	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
DL 49	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DR 49	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			

Permissible values: 1 to+9,999,999

Distance values for ranges BEE1 to 3 for positions 1 to 254
Data words DW 50 and DW 51 are for the distance value for BEE1.
Data words DW 52 and DW 53 are for the distance value for BEE2.
Data words DW 54 and DW 55 are for the distance value for BEE3.

	Binary representation								BCD representation							
Data byte	**Bit**								**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 50/52/54	0	0	0	0	0	0	0	0	0				0			
DR	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
50/52/54	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DL 51/53/55	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			
DR																

Permissible values:
- From 0 to 999,999 for a linear axis
- From 0 to 0.5·[final pos. of rotary axis] but not exceeding 999,999

Note: Distance for BEE1 distance for BEE2 distance for BEE3

Number of positions to be transferred during configuring

Data byte	**Bit**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DL 58	0	0	0	0	0	0	0	0
DR 58	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Permissible values: 0 to 254

Position number and position value for positions 1 to 254

In the tables below, the first word for a position entry is always identified by variable n. The first position entry begins at data word DW 60.

1st	position entry	:	DW 60	to	DW 62	(n=60)
2nd	position entry	:	DW 63	to	DW 65	(n=63)
3rd	position entry	:	DW 66	to	DW 68	(n=66)
						:
254th	position entry:		DW 819	to	DW 821	(n=819)

Position number

Binary representation

Data byte	Bit 7	6	5	4	3	2	1	0
DL n	0	0	0	0	0	0	0	0
DR n	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Permissible values: 1 to 254

Position value

	Binary representation								BCD representation							
Data byte	Bit 7	6	5	4	3	2	1	0	Bit 7	6	5	4	3	2	1	0
DL n+1	SE	SE	SE	SE	SE	SE	SE	SE	SG				10^6			
DR n+1	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	10^5				10^4			
DL n+2	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	10^3				10^2			
DR n+2	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^1				10^0			
	Negative values must be represented by the two's complement. SE=Sign extension								”1111” must be entered in the high-order nibble (SG) for a negative number.							

Permissible values:
- From - 9,999,999 to+9,999,999 for a linear axis
- From 0 to+[final pos. of the rotary axis - 1] for a rotary axis

10.23.2 The Configuring Function Block

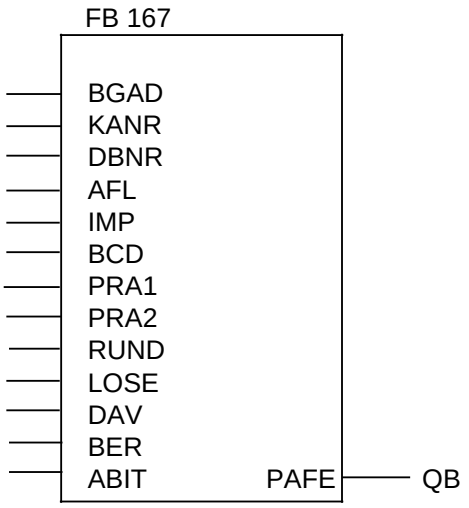
FB 167 (STRU.POS) Configures and initializes the IP 240 for ”positioning” mode

Functional description
The configuring FB first checks the input parameters and the length of the data block to be used for data interchange with the IP. It then transfers the general module data (machine-readable product designation of the module, FW and HW versions) from the IP to the data block, verifying its own compatibility with the firmware version as it does so. It then enters any errors detected during the startup test (Section 6.4) in the data block. Finally, the configuring data (parameters for FB 167) and the following data areas from the DB to the IP:

- Zero offset
- Final value (pos.) for the rotary axis
- Distance values for the switching and signalling ranges
- Position numbers and position values for positions 1 to 254.

Following error-free configuring of the channel, a mode identifier is entered in data byte DL 23.
If the channel is reconfigured, active outputs are reset and any interrupts pending for the channel cancelled.
Hardware, parameter assignment and data errors are flagged in the PAFE byte and described in detail in data words DW 8 to DW 10 and DW 13. Should an error occur, the addressed channel is not configured.

Invoking the function block
The configuring FB is invoked in the restart organization blocks.

STL	LAD/CSF
: JU FB 167 NAME : STRU.POS BGAD : KF KANR : KF DBNR : KF / KY AFL : KF IMP : KF BCD : KY PRA1 : KM PRA2 : KM RUND : KF LOSE : KF DAV : KF PAFE : QB BER : KF ABIT : KY	

Note

The data block number (DBNR) must be specified in KF format in the S5-115U and S5-150U and in KY format in the S5-135U and S5-155U.
The S5-115U requires no address space specification (BER), the S5-115U and S5-135U no ABIT parameter.

Table 10-28. Parameters for Configuring FB 167

NAME	Parameter type	Data type	Description
BGAD	D	KF	Module start address
KANR	D	KF	Channel number
DBNR	D	KF/KY	Data block number
AFL	D	KF	Resolution of encoder pulses
IMP	D	KF	Zero mark monitoring
BCD	D	KF	Number format
PRA1	D	KF	Allocation of interrupts
PRA2	D	KY	Allocation of interrupts
RUND	D	KM	Type of axis
LOSE	D	KM	Backlash compensation
DAV	D	KF	Switching performance of the IP outputs
PAFE	A	BY	Parameter assignment error byte
BER*	D	KF	Address space
ABIT**	D	KY	Signal change evaluation for interrupt processing with I/O byte PY 0

* Not required for FB 167 for the S5-115U
** Not required for FB 167 for the S5-115U and S5-135U

Parameters

BGAD: KF 128 to 240 Start address of the module, divisible by 16, in the P area
0 to 240 Start address of the module, divisible by 16, in the Q area

KANR: KF 1 Channel 1
2 Channel 2

DBNR:

Format	Description	Valid for
KF 3 to 255	Number of the data block created	S5-115U and S5-150U
KY x,y x=0 x=1 y=3 to 255	 Data block was created in the DB area Data block was created in the DX area Number of the data block created	S5-135U and S5-155U

AFL : KF 1 Single resolution of encoder pulses
2 Twofold resolution of encoder pulses
4 Fourfold resolution of encoder pulses

IMP : KF 0 No zero mark monitoring
10 Number of pulses between two zero marks divisible by 5 (without a remainder)
16 Number of pulses between two zero marks divisible by 4 (without a remainder)

BCD : KY x,y

	Number format
x /y=0	Binary
x /y=1	BCD

x determines the following values:
- Position values for positions 1 to 254
- Distance values for positions 1 to 254
- Final position of the rotary axis

y determines the following values:
- Position value for position 0
- Zero offset
- Actual value
- Final value

PRA1 : KM

0000 0000	Allocation of interrupts
0000 0000	
-	Bit n=1 An interrupt is triggered over the assigned status bit
0000 0000	
0000 1111	Bit n=0 No interrupt is triggered over the assigned status bit

Bit 0 : with negative-going edge of BEE1 (range BEE1 entered)
Bit 1 : with negative-going edge of BEE2 (range BEE2 entered)
Bit 2 : with negative-going edge of BEE3 (range BEE3 entered)
Bit 3 : with positive-going edge of MESE (actual pos. stored)

PRA2 : KM

0000 0000	Allocation of interrupts
0000 0000	
-	Bit n=1 An interrupt is triggered over the assigned status bit
0000 0000	
0011 1111	Bit n=0 No interrupt is triggered over the assigned status bit

Bit 0 : with positive-going edge of UEBL (counter in overrange)
Bit 1 : with positive-going edge of NPUE (zero mark error)
Bit 2 : with positive-going edge of DRBR (wirebreak)
Bit 3 : with positive-going edge of UEBS (old final value over- written)
Bit 4 : with positive-going edge of ZBEV (range BEE3 exited)
Bit 5 : with positive-going edge of RIUM (range BEE2 exited)

RUND : KF

0	Linear axis
1	Rotary axis

LOSE : KF

0	No backlash compensation
1	Backlash compensation

DAV : KF

0	IP outputs control the traversing speed, separate switching
1	IP outputs control the traversing speed, collective switching
2	IP outputs control the direction

PAFE : QB QB or FY (0 to 239) for flagging errors (Section 6.4)

BER : KF 0 Addressing in P area
1 Addressing in Q area

ABIT : KYx,y **x**=0 to 255 x>0 : The interrupt service OB is invoked on every signal change of the interrupt bit

x=0 : The interrupt service OB is invoked only when the interrupt bit goes from 0 to 1

y= 0 to 7 y : Interrupt bit in PY 0 set on switchbank S1

Note

Interrupts are not disabled in the configuring FBs. It must be ensured that these FBs cannot be interrupted in the S5-115U, S5-135U (by setting for interrupt servicing after every statement) and S5-155U (155U mode) by writing the STEP 5 program accordingly. Interrupts are disabled in the restart OBs.

Cycle on-load caused by configuring
Because configuring of a channel increases the module firmware's cycle time, you must write the STEP 5 program so that the other channel is in a safe wait state while a configuring FB is in progress.

Technical Specifications

Block number : 167

Block name : STRU. POS

AG	Library number	Call length/ Block length	CPU	Processing time [1]
S5-115U	P71200-S 5167-D-2	14 words/ 1159 words	941-7UA...	approx. 95 to 990 ms
			942-7UA...	approx. 48 to 565 ms
			943-7UA...	approx. 34 to 420 ms
			944-7UA...	approx. 14 to 204 ms
			941-7UB...	approx. 34 to 410 ms
			942-7UB...	
			943-7UB...	
			944-7UB...	approx. 14 to 170 ms
S5-135U/ S5-155U	P71200-S 9167-D-2	15 words/ 1152 words	922 from A9	approx. 23.5 to 320 ms
			928-3UA...	approx. 18 to 264 ms
			928-3UB...	approx. 13 to 161 ms
S5-150U	P71200-S 4167-D-1	16 words/ 1186 words		approx. 11.5 to 176 ms
S5-155U	P71200-S 6167-B-1	16 words/ 1197 words	946-3UA.../ 947-3UA...	approx. 10.5 to 130 ms

Nesting depth : 0

Subordinate blocks : keine

Reservations in data area : The data block specified in the DBNR parameter. The number of data words depends on the number of positions stored.

Flags used : MB 240 to 255

Reservations in system area : S5-135U BS 60 to 63
: S5-150U BS 150 to 153
: S5-155U BS 60 to 63

System commands : yes

[1] These execution times apply for an FB call following an IP 240 firmware cycle without data interchange. The execution time depends on the number of positions transferred (0 to 254).

10.23.3 The Control Function Block

FB 168 (STEU.POS) Control function block for ”positioning” mode

Functional Description
The control function block first checks to make sure that the DB has the correct identifier in DL 23 and that the channel was configured for ”positioning” mode. Then, depending on the parameters with which the FB was initialized, specific data areas are forwarded from the data block to the IP or read out from the IP and updated in the data block.

The following functions are possible:
- Read actual value, final value and status bits
- Write control bits and position number
- Write position data for position 0
- Read interrupt request bytes
- Write new position values for positions 1 to 254
- Write new zero offset
- Write new distance values for positions 1 to 254

Parameter assignment errors and data errors are flagged in the PAFE byte and described in detail in data words DW 8 to 10 and DW 13. When an error is detected, the selected function is not executed.

Indirect initialization
Indirect initialization means indirect specification of the data block number and the function number.

- Initializing the data block number
  You can initialize the DBNR by entering the data block number directly or by specifying ”0” or ”0,0” and opening the data block you want to use before invoking the FB.

- Initializing the function number
  You can initialize the FKT parameter by entering either ”0,0” or the number of the function you want to execute. If you enter FKT=0,0, FB 168 takes the function number that was entered in DW 19 of the data block.

Data byte	Bit 7	6	5	4	3	2	1	0	FKT: KY x,y
DL 19	0	0	2^5	2^4	2^3	2^2	2^1	2^0	FKT x
DR 19	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	FKT y

During configuring, FB 167 enters data in the data block which is needed by FB 168. If you want the control FB to use a different data block, you must copy the following data words to that block:
- DW 0
- DW 11 to 12
- DW 14 to 18
- DW 22 to 27
- DW 34
- DW 56 to 57

These data words should be copied in the restart routine immediately following configuring.

Invoking the control function block
The control FB is normally invoked in the cyclic program and in the interrupt service OBs.

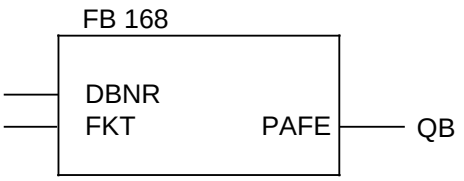
STL	LAD/CSF
: JU FB 168 NAME: STEU.POS DBNR: KF/KY FKT : KY PAFE : QB	

Table 10-29. Parameters for Control FB 168

Name	Parameter type	Data type	Description
DBNR	D	KF/KY	Data block number
FKT	D	KY	Function number
PAFE	Q	BY	Error byte

Parameters

DBNR:

Format	Description	Valid for
KF 0	Use the data block that has already been opened. In the S5-115U, this function is only available from CPU 943 onwards.	S5-115U and S5-150U
KF 3 to 255	Number of the data block to be opened instead	
KY x,y		S5-135U and S5-155U
x=0	Data block was created in DB area	
x=1	Data block was created in DX area	
y=0	Use the data block opened before the FB was called. x must always be ”0” in this case, regardless of where the DB was created.	
y=3 to 255	Number of the data block to be opened instead.	

Note

The standard function blocks use scratch flags and system data areas for handling data interchange with the IP 240 (Technical specifications for the FBs).
You must

- save these flags and system data areas at the beginning of the interrupt service routines for the S5-115U, S5-135U (when interrupt servicing enabled after each statement) and S5-155U (155U mode) and reload them at the end of these routines.
- save these flags and data areas in the restart routine (OB21/OB22) for the S5-135U (with preset restart mode) and the S5-150U and reload them at the end of this routine.

FKT : KY x,y

Format x	Format y	Description
0	0	Take function number (FKT) from DW 19.
1	-	Read actual value, feedback position number, status bits and final value.
20	0	Write control bits.
	1	Write control bits to disable the IP outputs. The FB sets control bit FREI (D36/8) to ”0”.
21	1 to 255	Write control bits and position number. y= Position number to be transferred y=255 Retain old position number The FB transfers the y entry to DR35 in the data block.
22	0	Write position data for position 0.
3	-	Read interrupt request bytes
41	1 to 255	Transfer position value for the yth entry in the DB. y= Entry to be transferred
42	1 to 255	Transfer position values for the yth and the (y+1)th entry in the DB. y= First entry to be transferred
5		Transfer zero offset
	0	Zero offset is relative, the FB sets the ADD bit (D45/0) to ”0”.
	>0	Zero offset is additive, the FB sets the ADD bit (D45/0) to ”1”.
6	-	Transfer distance values for positions 1 to 254

PAFE : QB Output or flag byte (0 to 239) to be used for flagging errors (Section 6.4).

Technical Specifications

Block number : 168

Block name : STEU. POS

AG	Library number	Call length/ Block length	CPU	Processing time[1] Function	1	20	21	22	3	41/42	5	6	
S5-115U	P71200-S 5168-D-2	5 words/ 830 words	941-7UA...	approx.	21	22	22	22.5	21	28.5	25.5	25	ms
			942-7UA...	approx.	9.6	8.4	9.0	10.5	8.8	10.5	9.6	10	ms
			943-7UA...	approx.	6.6	6.0	6.2	7.6	6.2	6.8	6.6	7.4	ms
			944-7UA...	approx.	2.3	2.0	2.9	2.8	1.9	2.3	2.0	2.7	ms
				approx.	2.3	2.0	2.9	2.8	1.9	2.3	2.0	2.7	ms
			941-7UB... 942-7UB... 943-7UB... 944-7UB...	approx.	6.4	6.0	6.2	7.4	6.0	6.6	6.4	7.4	ms
S5-135U/ S5-155U	P71200-S 9168-D-2	5 words/ 833 words	922 ab A9	approx.	4.3	4.8	4.8	5.3	5.0	6.2	5.3	5.8	ms
			928-3UA...	approx.	2.5	2.6	2.8	3.4	2.9	4.0	3.1	3.7	ms
			928-3UB...	approx.	2.4	2.1	2.1	3.0	2.2	3.0	2.2	3.0	ms
S5-150U	P71200-S 4168-D-1	5 words/ 805 words		approx.	1.0	0.8	1.0	1.7	1.0	1.7	1.0	1.8	ms
S5-155U	P71200-S 6168-B-1	5 words/ 947 words	946-3UA.../ 947-3UA...	approx.	1.0	0.9	1.8	2.5	1.0	1.6	1.4	1.7	ms

Nesting depth : 0

Subordinate blocks : S5-115U OB160 (only CPUs to -7UB...)
S5-135U OB122
S5-155U OB91, OB122

Reservations in data area : Data block specified in the DBNR parameter. The number of data words depends on the number of positions stored.

Flags : MB 240 to 255

System area : S5-135U BS 60 to 63
: S5-150U BS 150 to 153
: S5-155U BS 60 to 63

System operations : yes

[1] The execution times shown above apply for an FB call following an IP 240 firmware cycle without data interchange. Note that
- when data are read out from the IP, no further data interchange is possible in that firmware cycle.
- when new data are written to the IP, no further data interchange is possible in that firmware cycle, nor in the next cycle.

10.24 Sample Program for Processing Data Words with a Data Word Number Exceeding 255

If a data block exceeds a length of 256 data words, those data words with a data word number exceeding 255 must be processed using supplementary STEP 5 operations (system operations). The sample programs below are intended to help you work with these data words.

Function:
The PLC-specific ”L/T DWX” function blocks are used to load and transfer three data words with word numbers greater than 255; these data words cannot be addressed using STEP 5 operations ”L DW x” and ”T DW x”.

> **Note**
>
> The following sample programs do not check to see whether the specified data block has been created or is of sufficient length. Should this be the case, the S5 CPU may go to STOP.

Descriptions of the identifiers:

```
DBNR - D KF  DATA BLOCK NUMBER

DWNR - I  W  1st DATA WORD TO BE READ OR WRITTEN

L/T  - I BI  ON A ”0” SIGNAL, THE CONTENTS OF THE THREE DWs ARE OUTPUT TO
             ”         DWN” - ”DWN2”
             ON A ”1” SIGNAL, THE VALUES IN ”DWN” - ”DWN2” ARE TRANSFERRED
                       TO THE DATA BLOCK

DWN  - I  W  VALUE FROM/FOR DATA WORD ”DWNR”
             (DL=FREE, DR=POSITION NUMBER)

DWN1 - I  W  VALUE FROM/FOR DATA WORD ”DWNR”+1
             (POSITION VALUE: SG AND DECADES 10^4 - 10^6 OR 2^16 - 2^23)

DWN2 - I  W  VALUE FROM/FOR DATA WORD ”DWNR”+2
             (POSITION VALUE: DECADES 10^0 - 10^3 OR 2 ^ 0 - 2 ^ 15)
```

```
*************************
SAMPLE PROGRAM FOR S5-115U
*************************

NAME :L/T DWX
ID   :DBNR      I/Q/D/B/T/C: D KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DWNR      I/Q/D/B/T/C: I BI/BY/W/D: W
ID   :L/T       I/Q/D/B/T/C: I BI/BY/W/D: BI
ID   :DWN       I/Q/D/B/T/C: I BI/BY/W/D: W
ID   :DWN1      I/Q/D/B/T/C: I BI/BY/W/D: W
ID   :DWN2      I/Q/D/B/T/C: I BI/BY/W/D: W

0017      :L   KH E400                        BASE ADDRESS FOR MODULE
0019      :LW  =DBNR                          ADDRESS LIST DBs (115U)
001A      :SLW      1
001B      :+F
001C      :LIR      0                         LOAD ADDRESS OF 1ST DW (DW0)
001D      :L   =DWNR                          SOURCE/TARGET DATA WORD NUMBER
001E      :SLW      1                         TIMES 2 (BYTE MACHINE)
001F      :+F                                 COMPUTE 1ST DW ADDRESS
0020      :A   =L/T                           LOAD/TRANSFER VALUES
0021      :JC  =TIR
0022      :LIR      2                         LOAD ACCUM2 WITH VALUE FROM DW N
0023      :TAK                                FETCH VALUE IN ACCUM1
0024      :T   =DWN                           OUTPUT VALUE
0025      :TAK                                LOAD ACCUM1 WITH DW ADDRESS
0026      :ADD BN +2                          OFFSET OF +2 TO DW ADDRESS
0027      :LIR      2                         LOAD ACCUM2 WITH VALUE FROM DW N+1
0028      :TAK                                FETCH VALUE IN ACCUM1
0029      :T   =DWN1                          AND OUTPUT
002A      :TAK                                .
002B      :ADD BN +2                          .
002C      :LIR      2                         .
002D      :TAK
002E      :T   =DWN2
002F      :BEU
0030 TIR  :L   =DWN                           LOAD VALUE FOR DW N
0031      :TAK                                LOAD ACCUM1 WITH DW ADDRESS
0032      :TIR      2                         TRANSFER VALUE TO DW N
0033      :ADD BN +2                          OFFSET OF +2 TO DW ADDRESS
0034      :L   =DWN1                          LOAD VALUE FOR DW N+1
0035      :TAK                                LOAD ACCUM1 WITH DW ADDRESS
0036      :TIR      2                         TRANSFER VALUE TO DW N+1
0037      :ADD BN +2                          .
0038      :L   =DWN2                          .
0039      :TAK                                .
003A      :TIR      2
003B      :BE
```

```
**********************************
SAMPLE PROGRAM FOR S5-135U AND 150U
**********************************

ADDRESS REQUIRED IN PROGRAM DEPENDS ON
PLC TYPE AND DATA BLOCK TYPE:

    S5-135U - DB - DF00 HEX
            - DX - DE00 HEX

    S5-150U - DB - DBBE HEX

=====================================================

NAME :L/T DWX
ID   :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DWNR      I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :L/T       I/Q/D/B/T/C: I  BI/BY/W/D: BI
ID   :DWN       I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :DWN1      I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :DWN2      I/Q/D/B/T/C: I  BI/BY/W/D: W

0017      :K   KH DF00                        (DF00 FOR DB/135U)
0019      :LW  =DBNR                          (DE00 FOR DX/135U)
001A      :+F                                 (DBBE FOR DB/150U)
001B      :LIR      1                         LOAD ADDRESS OF 1ST DW (DW0)
001C      :L   =DWNR                          SOURCE/TARGET DATA WORD NUMBER
001D      :+F                                 COMPUTE 1ST DW ADDRESS
001E      :A   =L/T                           LOAD/TRANSFER VALUES
001F      :JC  =TIR
0020      :LIR      3                         LOAD ACCUM2 WITH VAL.FROM DW N
0021      :TAK                                FETCH VALUE IN ACCUM1
0022      :T   =DWN                           OUTPUT VALUE
0023      :TAK                                LOAD ACCUM1 WITH DW ADDRESS
0024      :ADD BN +1                          OFFSET OF +2 TO DW ADDRESS
0025      :LIR      3                         LOAD ACCUM2 W. VAL.FRO: DW N+1
0026      :TAK                                FETCH VALUE IN ACCUM1
0027      :T   =DWN1                          AND OUTPUT
0028      :TAK                                .
0029      :ADD BN +1                          .
002A      :LIR      3                         .
002B      :TAK
002C      :T   =DWN2
002D      :BEU
002E TIR  :L   =DWN                           LOAD VALUE FOR DW N
002F      :TAK                                LOAD DW ADDR. INTO ACCUM1
0030      :TIR      3                         TRANSFER VALUE TO DW N
0031      :ADD BN +1                          OFFSET OF +2 TO DW ADDRESS
0032      :L   =DWN1                          LOAD VALUE FOR DW N+1
0033      :TAK                                LOAD DW ADDR. INTO ACCUM1
0034      :TIR      3                         TRANSFER VALUE TO DW N+1
0035      :ADD BN +1                          .
0036      :L   =DWN2                          .
0037      :TAK                                .
0038      :TIR      3
0039      :BE
```

```
*************************
SAMPLE PROGRAM FOR S5-155U
*************************

THE ADDRESS REQUIRED IN THE PROGRAM
DEPENDS ON THE DATA BLOCK TYPE:

   S5-155U - DB - EEC00 HEX
           - DX - EEE00 HEX

==========================================

NAME :L/T DWX
ID   :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DWNR      I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :L/T       I/Q/D/B/T/C: I  BI/BY/W/D: BI
ID   :DWN       I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :DWN1      I/Q/D/B/T/C: I  BI/BY/W/D: W
ID   :DWN2      I/Q/D/B/T/C: I  BI/BY/W/D: W

0017      :L   DH   000E EC00               BLOCK ADDRESS LIST DBs
001A      :LW  =DBNR                        (EEE00 FOR DX BLOCKS)
001B      :+D
001C      :LIR      1                       LOAD ADDRESS OF 1ST DW (DW0)
001D      :SLD     16
001E      :RRD     12
001F      :L   =DWNR                        SOURCE/TARGET DATA WORD NUMBER
0020      :+D                               COMPUTE 1ST DW ADDRESS
0021      :MAB
0022      :A   =L/T                         LOAD/TRANSFER VALUES
0023      :JC  =TIR
0024      :LRW    +0                        LOAD ACCUM1 WITH VAL.FROM DW N
0026      :T   =DWN                          AND OUTPUT
0027      :LRW    +1                        LOAD ACCUM1 W. VAL.FROM DW N+1
0029      :T   =DWN1                         AND OUTPUT
002A      :LRW    +2                        LOAD ACCUM1 W. VAL.FROM DW N+2
002C      :T   =DWN2                         AND OUTPUT
002D      :BEU
002E TIR  :L   =DWN                         LOAD VALUE INTO ACCUM1
002F      :TRW    +0                        AND TRANSFER TO DW N
0031      :L   =DWN1                        LOAD VALUE INTO ACCUM1
0032      :TRW    +1                        AND TRANSFER TO DW N+1
0034      :L   =DWN2                        LOAD VALUE INTO ACCUM1
0035      :TRW    +2                        AND TRANSFER TO DW N+2
0037      :BE
```

10.25 Example: Removing Parts from a Die-Casting Machine

Finished parts are to be taken from a die-casting machine and deposited at various positions.
This example concentrates on positioning of one of the three axes.
When the setpoint is reached, an interrupt is generated, thus enabling a gripper.
The traversing speed (rapid traverse or creep speed) is set directly via the IP's digital outputs.
The IP 240 determines the direction of travel. The S5 CPU queries the IP as to the direction and forwards it to the relevant outputs. The drive can start only in the specified direction, which is used as enable.

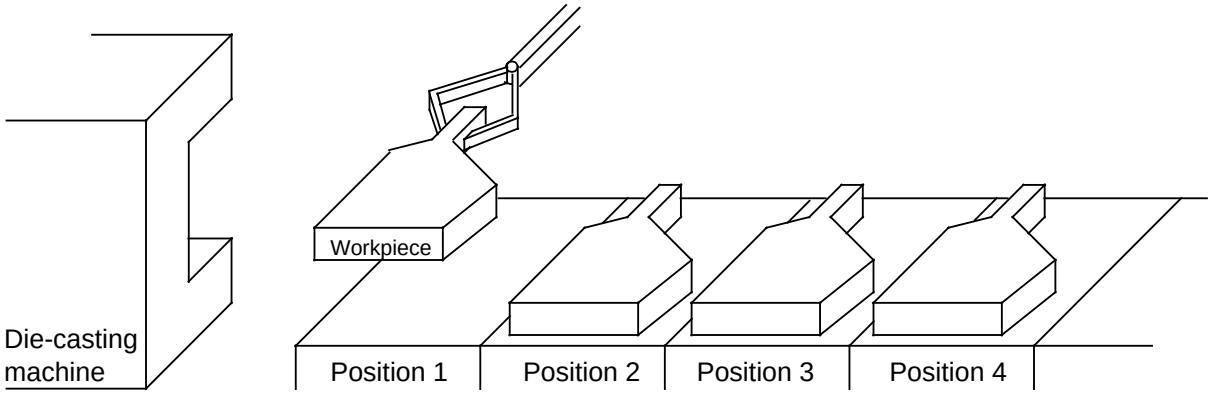


Fig. 10-33. Positioning a Workpiece to a Specified Position

Functional description
Channel 1 on the IP 240 is configured and the auxiliary flags reset in the programmable controller's restart routine.
The cyclic program comprises several segments, as can be seen from the "Function sequence" diagram.

1. Power-up
   A reference point is automatically approached (FB 31) on power-up. The limit switch, which limits the negative traversing range, is used as preliminary contact signal.
2. Approaching the home position
   Following termination of the reference point approach, the position whose number was stored in DR 11, DB 100 (home position) is approached.
   Positioning begins when the ”START” input is set.
3. Approaching the removal position
   The position number stored in DL 11 (DB 100) (removal position) is approached and a gripper activated (gripper closes) which picks up the workpiece.
4. Depositing a workpiece
   The workpiece which the gripper took from the machine is brought to the specified position and ejected (gripper opens). The eject positions are stored in DR 12 (1st position) to DL 12 (last position).
   Steps 3 and 4 are repeated until a workpiece has been deposited at each position.

Faults
Any faults occurring while the main switch is on are signalled by a hooter.

Flags, inputs, outputs, timers and DBs

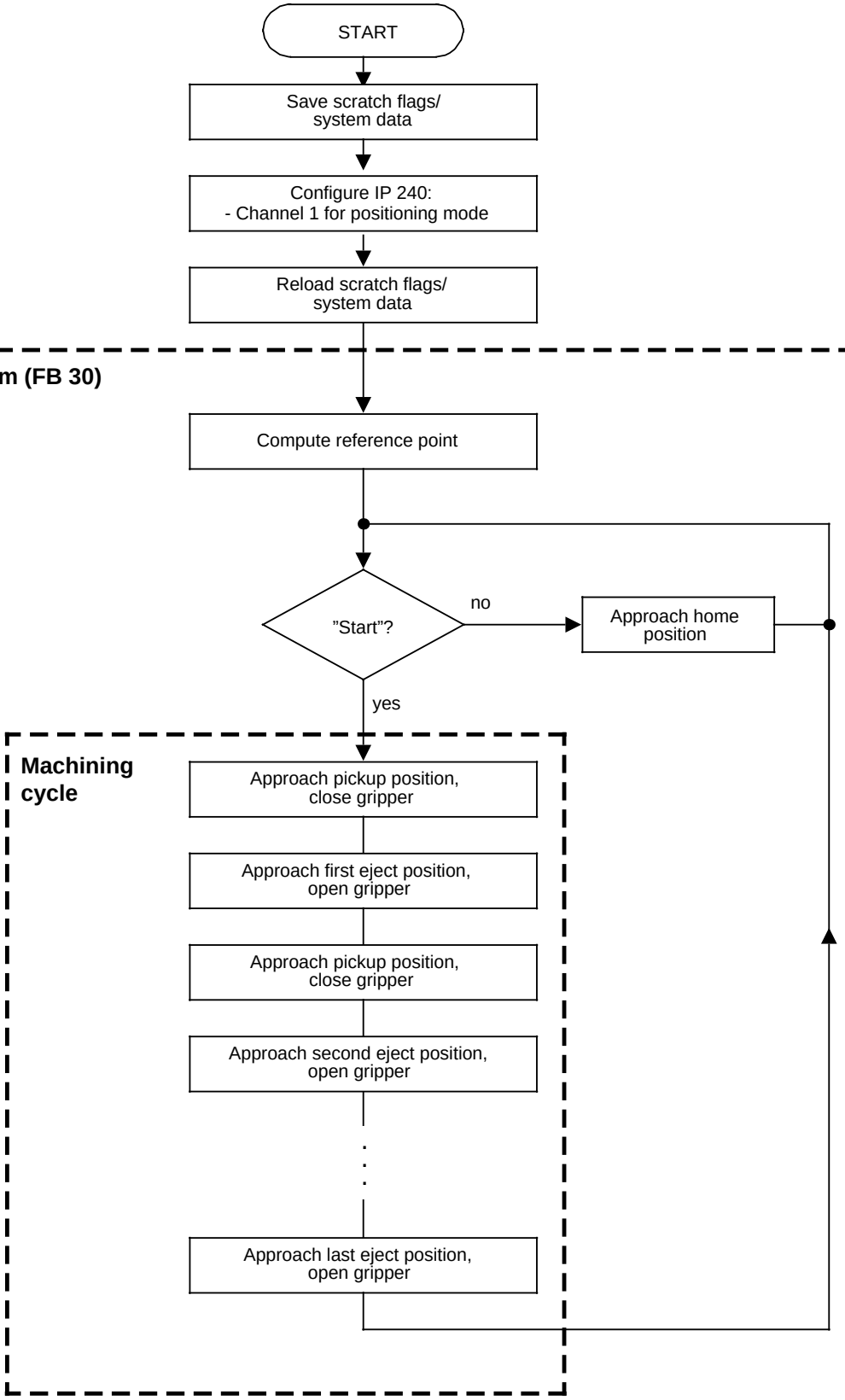
OPERAND	SYMBOL	COMMENTARY
F 0.0	RLO0	FLAG FOR "0" SIGNAL
F 0.1	RLO1	FLAG FOR "1" SIGNAL
FY 60	NPOS	NUMBER OF NEXT POSITION TO BE APPROACHED
FY 61	RESPONSE	RESPONSE ON REACHING POSITION
F 61.0	RESP01	OPEN GRIPPER
F 61.1	RESP02	CLOSE GRIPPER
F 61.2	F 61.2	--
F 61.3	F 61.3	--
F 61.4	F 61.4	--
F 61.5	F 61.5	--
F 61.6	F 61.6	--
F 61.7	F 61.7	--
FY 62	CNTL	CONTROL BITS (DL36)
F 62.0	FREI	CONTROL BIT
F 62.1	HAND	CONTROL BIT
F 62.2	DA1S	CONTROL BIT
F 62.3	DA2S	CONTROL BIT
F 62.4	HASY	CONTROL BIT
F 62.5	SOSY	CONTROL BIT
F 62.6	ZYSY	CONTROL BIT
F 62.7	AMSK	CONTROL BIT
FY 63	STATBITS	STATUS BITS (DR29)
F 63.0	SYNC	STATUS BIT
F 63.1	RICH	STATUS BIT
F 63.2	BEE1	STATUS BIT
F 63.3	BEE2	STATUS BIT
F 63.4	BEE3	STATUS BIT
F 63.5	MESE	STATUS BIT
F 63.6	DA1	STATUS BIT
F 63.7	DA2	STATUS BIT
FY 64	STATUS	STATUS FROM POSITIONING PROG (FB10)
F 64.0	POSACTIV	POSITIONING IN PROGRESS
F 64.1	POSREADY	POSITION REACHED, RESPONSES TRIGGERED
F 64.2	REFACTIV	REFERENCE POINT APPROACH IN PROGRESS
F 64.3	REFEND	REFERENCE POINT APPROACH TERMINATED
F 64.4	F 64.4	--
F 64.5	MACHCYC	MACHINING CYCLE IN PROGRESS
F 64.6	AUXF01	AUXILIARY/SCRATCH FLAG
F 64.7	FAULT	GROUP ERROR FLAG (-> FLAG BYTE 65)

OPERAND	SYMBOL	COMMENTARY
FY 65	ERROR	REASON FOR SETTING GROUP ERROR FLAG (F 64.7)
F 65.0	ERR00	REF. POINT APPROACH TERM. WITHOUT SYNC
F 65.1	ERR01	NOT ENOUGH DISTANCE BETW. ACTVAL AND SETPOINT
F 65.2	ERR02	TARGET RANGE NOT REACHED
F 65.3	ERR03	TARGET RANGE EXITED (ZBV)
F 65.4	ERR04	PERM. POSITIONING TIME EXCEEDED
F 65.5	ERR05	INTERRUPTS DRB, NPU, OVF
F 65.6	ERR06	ACTVAL NO LONGER SYNCHRONIZED
F 65.7	ERR07	PAFE GROUP ERROR (-> FY200)
FY 66	FBPOS	FEEDBACK POS. NUMBER (DR28)
FY 67	EJECTPOS	NEXT EJECT POS. TO BE APPROACHED
FW 68	INTCH1	INTERR. REQUEST BYTES F. CHANNEL 1
F 68.0	UEB	IR COUNTER IN OVERRANGE
F 68.1	NPU	IR ZERO MARK ERROR
F 68.2	DRB	IR WIREBREAK/SHORT-CIRCUIT
F 68.3	UBS	IR FINAL VALUE OVERWRITTEN
F 68.4	ZBV	IR TARGET RANGE (BEE3) EXITED
F 68.5	RIU	IR CUT-OFF RANGE (BEE2) EXITED
F 68.6	F 68.6	--
F 68.7	F 68.7	--
F 69.0	F 69.0	--
F 69.1	RIC	STATUS FLAG
F 69.2	BE1	IR BEE1 ENTERED
F 69.3	BE2	IR BEE2 ENTERED
F 69.4	BE3	IR BEE3 ENTERED
F 69.5	MES	IR FINAL VALUE STORED
F 69.6	F 69.6	--
F 69.7	F 69.7	--

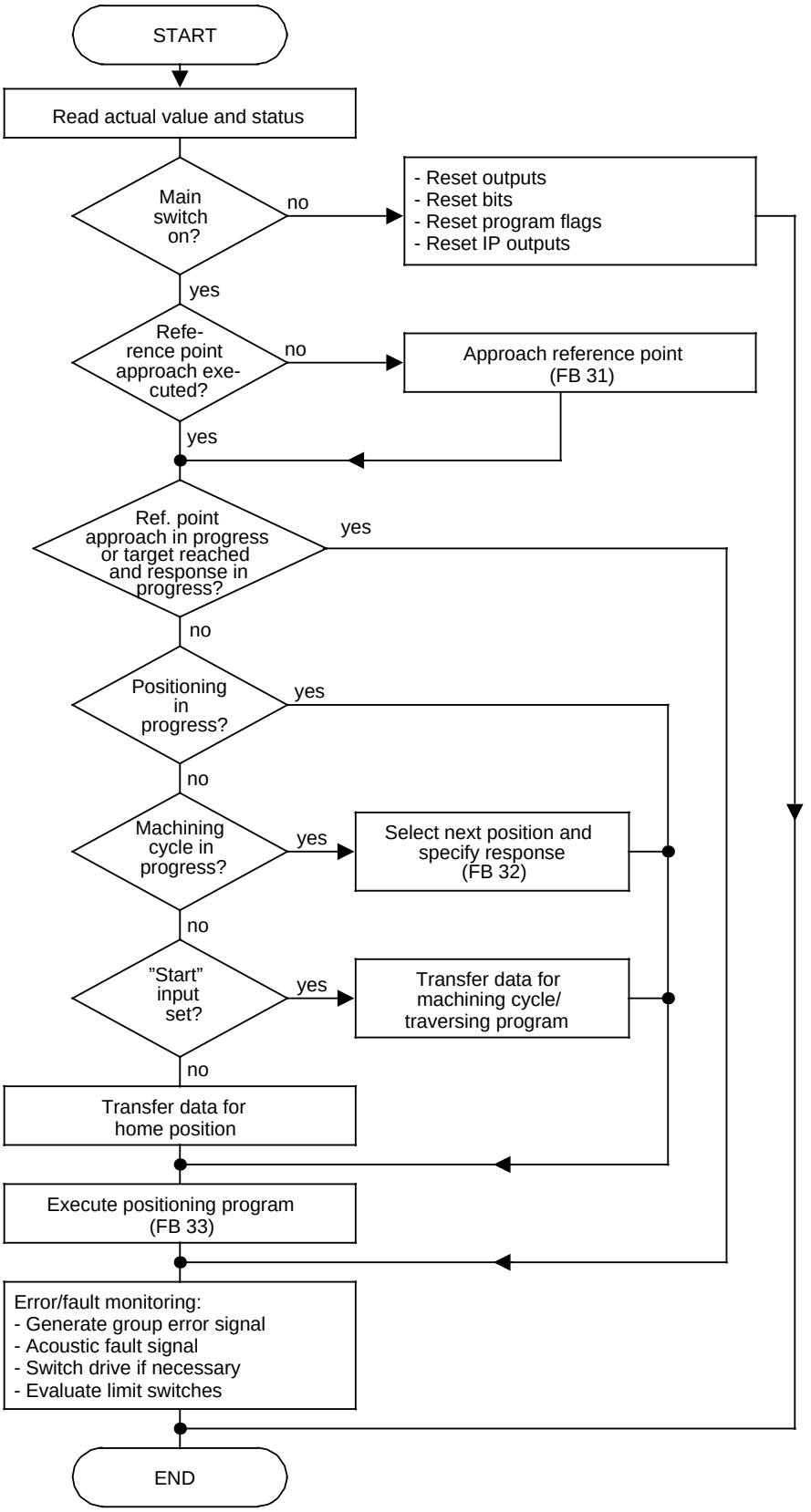
OPERAND	SYMBOL	COMMENTARY
FY 200	PAFE	CONTENTS SEE INSTR. MAN. SEC. 6.4
T 1	POSTIMER	WATCHDOG TIMER FOR POSITIONING
T 2	STOPTIMER	TIMER FOR MOTOR DECELERATION
T 3	REFTIMER	DELAY TIME FOR ZERO MARK AFTER PRELIM. CONTACT
T 4	STRTCLK	CLOCK PULSE FOR ACOUSTIC LIMIT SWITCH
T 5	STOPCLK	CLOCK PULSE FOR ACOUSTIC LIMIT SWITCH
Q 4.0	POSDIR	OUTPUT FOR DIRECTION
Q 4.1	NEGDIR	OUTPUT FOR DIRECTION
Q 4.2	HOOTER	ACOUSTIC FAULT SIGNAL
Q 5.0	OPENGR	OUTPUT FOR OPEN GRIPPER
Q 5.1	CLOSGR	OUTPUT FOR CLOSE GRIPPER
Q 6.0	INSIGNAL	PRELIM. CONTACT SIGNAL FOR CHANNEL 1 (INVERSE OF I 33.1)
I 32.0	MAINSW	MAIN SWITCH: DRIVE ENABLE
I 32.1	START	START OF POSITIONING PROGRAM
I 33.0	ENDPOS	LIMIT SWITCH FOR POSITIVE DIRECTION
I 33.1	ENDNEG	LIMIT SWITCH FOR NEGATIVE DIRECTION
I 33.2	GRUP	GRIPPER IN HOME POS. (UP)
I 33.3	GRDOWN	GRIPPER IN PICKUP/EJECT POS. (DOWN)
DB 100	DATA1	TRAVERSING DATA/ERROR MESSAGES
DW 0	DW0	RESTART ERROR FROM FB 167 (DW10)
DW 1	DW1	RESTART ERROR FROM FB 167 (DW13)
DR 11	HOMEPOS	POSITION NUMBER FOR HOME POSITION
DL 11	MACHPOS	POSITION NUMBER FOR EJECT POS.
DR 12	DR12	FIRST EJECT POSITION
DL 12	DL12	LAST EJECT POSITION
DB128	DBCH1	DB FOR CHANNEL 1

Functional sequence:

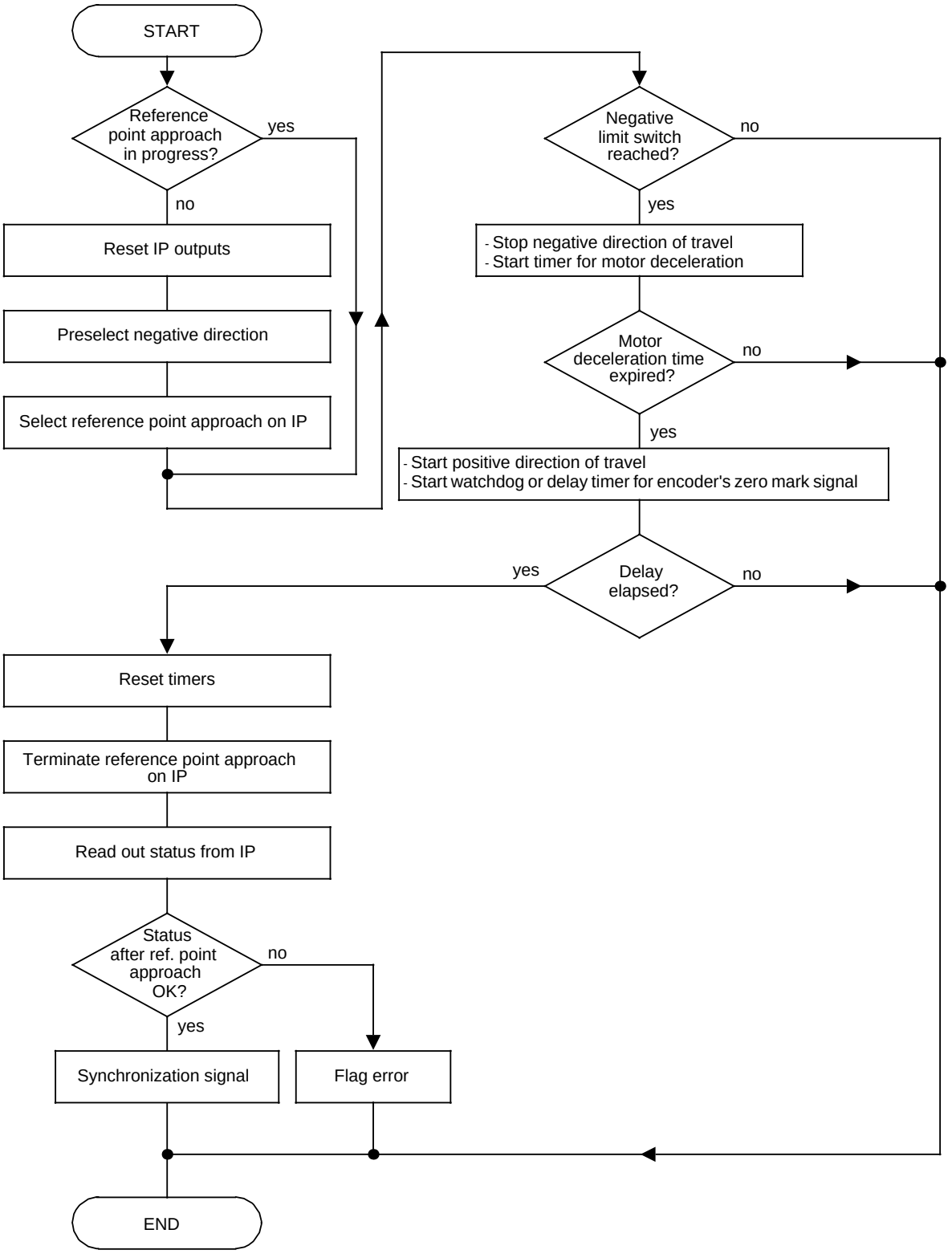
Restart routine (FB 20)



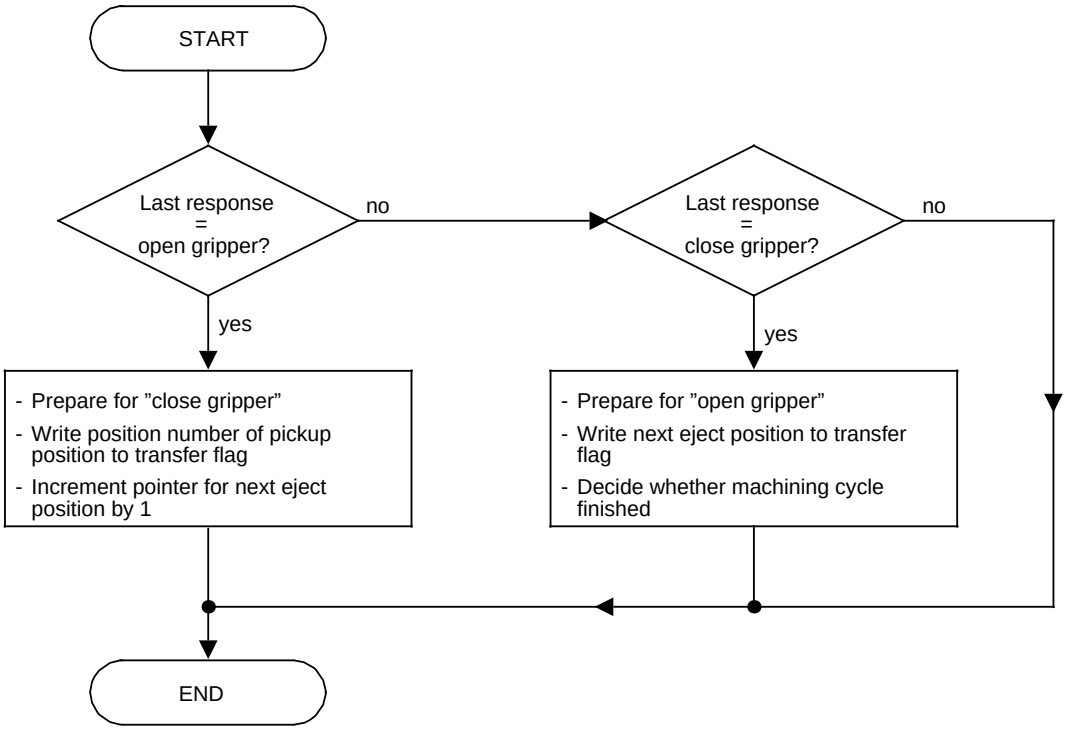
Cyclic program for x axis (FB 30)



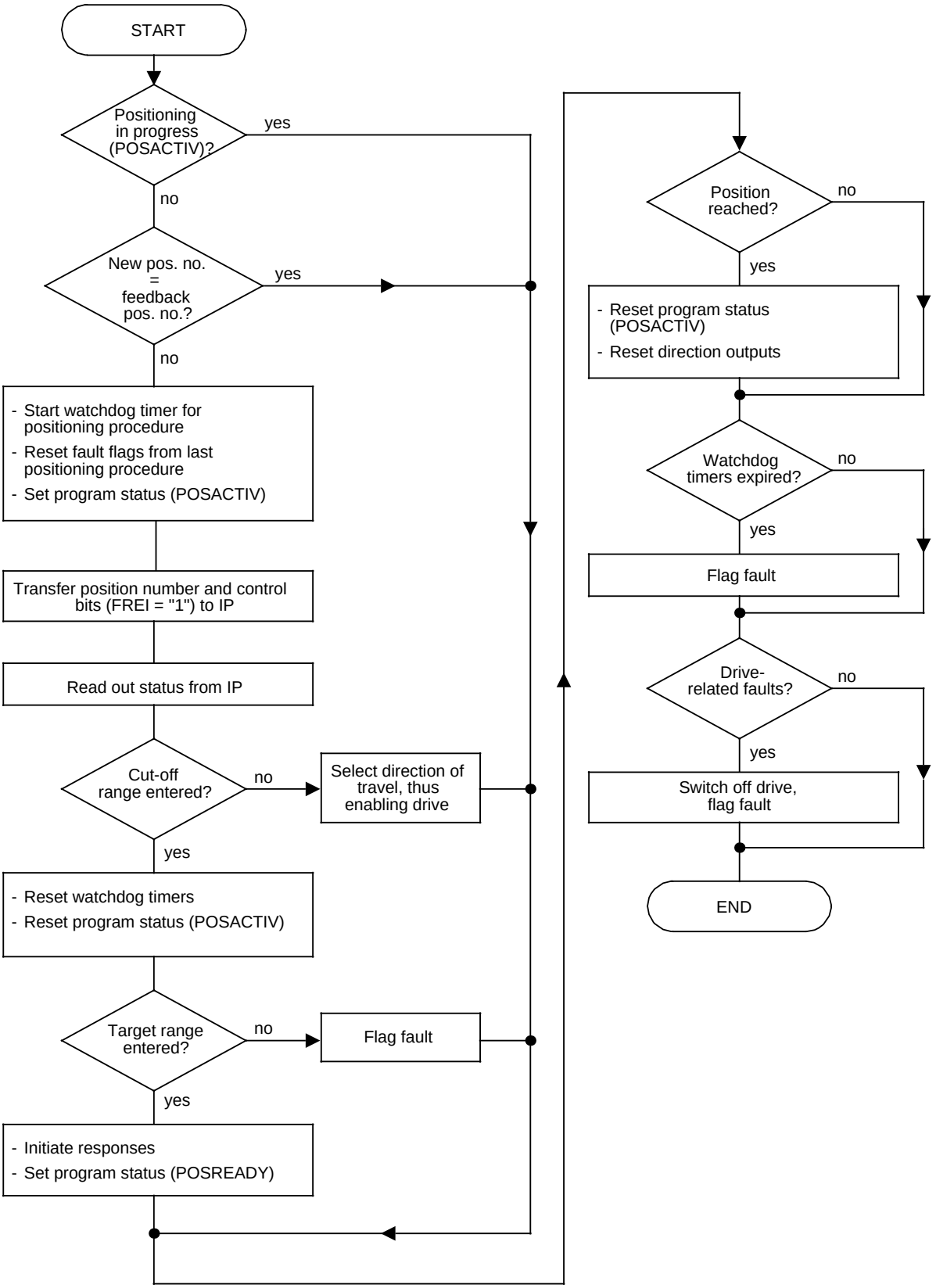
Reference point approach FB 31



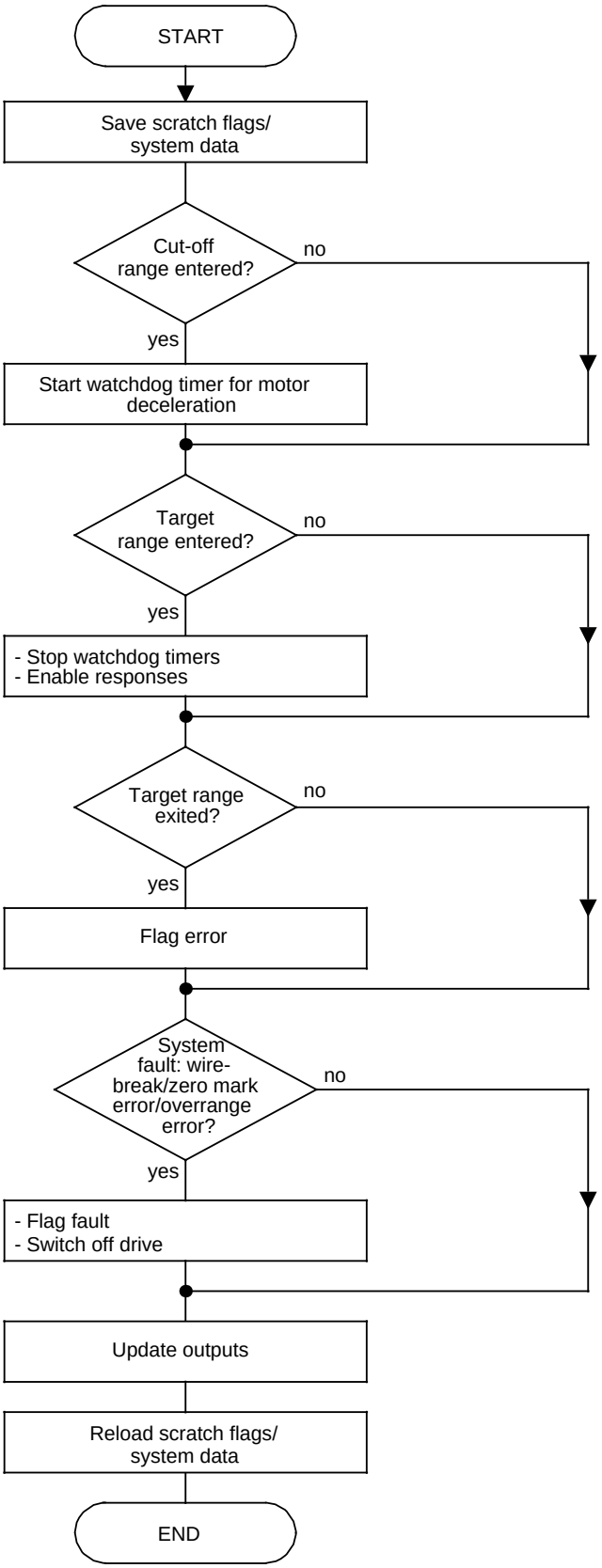
Select next position (FB 32)



Select and approach position (FB 33)



Interrupt service routine for x axis (FB 34)



```
DB100
                        TRAVERSING DATA
##################################################
#                                                #
#  DATA BLOCK WITH TRAVERSING DATA FOR CHANNEL 1 #
#                                                #
##################################################

DW  0 - ERROR FLAGGED IN RESTART ROUTINE BY FB167 (DB128/DW10)
DW  1 - ERROR FLAGGED IN RESTART ROUTINE BY FB167 (DB128/DW13)

DR 11 - POSITION NUMBER FOR HOME POSITION
DL 11 -    II      II    II  II  POSITION
DR 12 -    II      II    II  II  POSITION
DL 12 -    II      II    II  II  POSITION

     0:     KH = 0000;                        DW10 FROM DB128 IN RESTART ROUTINE
     1:     KH = 0000;                        DW13  II   II   II   II     II
     2:     KH = 0000;
     3:     KH = 0000;
     4:     KH = 0000;
     5:     KH = 0000;
     6:     KH = 0000;
     7:     KH = 0000;
     8:     KH = 0000;
     9:     KH = 0000;
    10:     KH = 0000;
    11:     KY = 008,002;                     PICKUP / HOME POSITION
    12:     KY = 006,004;                     LAST / FIRST EJECT POSITION
    13:     KH = 0000;
    14:     KH = 0000;
    15:     KH = 0000;
    16:     KH = 0000;
    17:     KH = 0000;
    18:     KH = 0000;
    19:     KH = 0000;
    20:     KH = 0000;                        ) SCRATCH FLAGS - INTERRUPT SERVICE
    21:     KH = 0000;                        ) ROUTINE (115/135/155U)
    22:     KH = 0000;                        )
    23:     KH = 0000;                        )
    24:     KH = 0000;                        )
    25:     KH = 0000;                        )
    26:     KH = 0000;                        )
    27:     KH = 0000;                        )
    28:     KH = 0000;
    29:     KH = 0000;
    30:     KH = 0000;                        ) SCRATCH FLAGS - RESTART ROUTINE
    31:     KH = 0000;                        ) (135/150U)
    32:     KH = 0000;                        )
    33:     KH = 0000;                        )
    34:     KH = 0000;                        )
    35:     KH = 0000;                        )
    36:     KH = 0000;                        )
    37:     KH = 0000;                        )
    38:     KH = 0000;
    39:     KH = 0000;
    40:     KH = 0000;                        ) RS DATA - INTERRUPT SERVICE
    41:     KH = 0000;                        ) ROUTINE (135/155U)
    42:     KH = 0000;                        )
    43:     KH = 0000;                        )
    44:     KH = 0000;
    45:     KH = 0000;                        ) RS DATA - RESTART ROUTINE
    46:     KH = 0000;                        ) (135/150U)
    47:     KH = 0000;                        )
    48:     KH = 0000;                        )
    49:     KH = 0000;
    50:
```

```
DB128

    0:     KH = 0000;
    1:     KS ='      ';                  MACHINE-READABLE PRODUCT DESIGNATION
    4:     S  ='      ';                  FIRMWARE VERSION
    7:     KS ='  ';                      HARDWARE VERSION
    8:     KH = 0000;                     ERROR NO. 1 FROM IP
    9:     KH = 0000;                     ERROR NO. 2 FROM IP
   10:     KH = 0000;                     ERROR NO. 3 FROM IP
   11:     KH = 0000;
   12:     KH = 0000;
   13:     KH = 0000;                     PAFE NIBBLES
   14:     KH = 0000;
   15:     KH = 0000;
   16:     KH = 0000;
   17:     KH = 0000;
   18:     KH = 0000;
   19:     KH = 0000;                     INDIRECT INITIALIZATION
   20:     KH = 0000;                     INTERRUPT BYTES CHANNEL 1
   21:     KH = 0000;                     INTERRUPT BYTES CHANNEL 2
   22:     KH = 0000;
   23:     KY = 000,000;                  MODE / DBNR
   24:     KH = 0000;
   25:     KH = 0000;
   26:     KH = 0000;
   27:     KH = 0000;
   28:     KY = 000,000;                  FEEDBACK POSITION NUMBER
   29:     KM = 00000000 00000000;        STATUS BITS
   30:     KH = 0000;                     ] ACTUAL VALUE
   31:     KH = 0000;                     ]
   32:     KH = 0000;                     ) FINAL COUNT (ZYSY)
   33:     KH = 0000;                     )
   34:     KH = 0000;
   35:     KH = 0000;                     NEW POS. NO.
   36:     KM = 00000000 00000000;        CONTROL BITS
   37:     KH = 0000;                     ) POS. VALUE      )  FOR POS 0
   38:     KH = 0000;                     )                 )
   39:     KH = 0000;                     ] BEE1            )
   40:     KH = 0000;                     ]                 )
   41:     KH = 0000;                     ) BEE2            )
   42:     KH = 0000;                     )                 )
   43:     KH = 0000;                       BEE3            )
   44:     KH = 0000;                     CONTROL BIT: GAUE )
   45:     KH = 0000;                     CONTROL BIT: ADD
   46:     KH = 0000;                     ] ZERO OFFSET VALUE
   47:     KH = 0000;                     ]
   48:     KH = 0000;                     ) MODULO VALUE FOR
   49:     KH = 0000;                     )   ROTARY AXIS
   50:     KH = 0004;                     ]  BEE1 f. POS 1- 254
   51:     KH = 0000;                     ]
   52:     KH = 0000;                     )  BEE2 f. POS 1- 254
   53:     KH = 0400;                     )
   54:     KH = 0000;                     ]  BEE3 f. POS 1- 254
   55:     KH = 0200;                     ]
   56:     KH = 0000;                     UNASSIGNED
   57:     KH = 0000;                     UNASSIGNED
   58:     KY = 000,015;                  NO. OF POSITIONS
   59:     KH = 0000;                     UNASSIGNED
   60:     KH = 0001;                       1ST POS. NO.
   61:     KH = 0015;                     ] 1ST VALUE
   62:     KH = 0000;                     ]
   63:     KH = 0002;                       2ND POS. NO.
   64:     KH = 0010;                     ] 2ND VALUE
   65:     KH = 0000;                     ]
   66:     KH = 0003;                       3RD POS. NO.
   67:     KH = 0020;                     ] 3RD VALUE
   68:     KH = 0000;                     ]
```

```
 69:     KH = 0004;                    4TH POS. NO.
 70:     KH = 0025;                  ] 4TH VALUE
 71:     KH = 0000;                  ]
 72:     KH = 0005;                    5TH POS. NO.
 73:     KH = 0000;                  ] 5TH VALUE
 74:     KH = 0000;                  ]
 75:     KH = 0006;                    6TH POS. NO.
 76:     KH = 0004;                  ] 6TH VALUE
 77:     KH = 0000;                  ]
 78:     KH = 0007;                    7TH POSITION
 79:     KH = 0030;
 80:     KH = 0000;
 81:     KH = 0008;                    8TH POSITION
 82:     KH = 0050;
 83:     KH = 0000;
 84:     KH = 0009;                    9TH POSITION
 85:     KH = 0030;
 86:     KH = 5000;
 87:     KH = 000A;                   10TH POSITION
 88:     KH = 0002;
 89:     KH = 0000;
 90:     KH = 000B;                   11TH POSITION
 91:     KH = 0051;
 92:     KH = 0000;
 93:     KH = 000C;                   12TH POSITION
 94:     KH = 0000;
 95:     KH = 0000;
 96:     KH = 000D;                   13TH POSITION
 97:     KH = F020;
 98:     KH = 0000;
 99:     KH = 000E;                   14TH POSITION
100:     KH = F040;
101:     KH = 0500;
102:     KH = 000F;                   15TH POSITION
103:     KH = F250;
104:     KH = 0000;
105:
```

```
FB 20

NETWORK 1      0000          GENERATE LOG. "0" AND "1"

####################################
#                                  #
# RESTART PROGRAM CONFIGURE AXIS 1 #
#                                  #
####################################


NAME :ANLAUF

0005      :A   F    0.0  -RLO0
0006      :R   F    0.0  -RLO0
0007      :AN  F    0.1  -RLO1
0008      :S   F    0.1  -RLO1
0009      :***

F    0.0 = RLO0                    FLAG FOR "0" SIGNAL
F    0.1 = RLO1                    FLAG FOR "1" SIGNAL

NETWORK 2    000A          SAVE SCRATCH FLAGS / RS DATA

000A      :                                 ---------------------------------
000B      :L   FW 240                       SAVE FLAGS 240-255
000C      :T   DW  30                       (SEE TECH. SPECS. FOR FB)
000D      :L   FW 242                       REQUIRED ONLY FOR 150U
000E      :T   DW  31                       AND FOR 135U WITH PRESET. OF
000F      :L   FW 244                       RESTART MODE IN DX0
0010      :T   DW  32                       (AUTO. WARM RESTART ON
0011      :L   FW 246                       POWER-UP)
0012      :T   DW  33
0013      :L   FW 248
0014      :T   DW  34
0015      :L   FW 250
0016      :T   DW  35
0017      :L   FW 252
0018      :T   DW  36
0019      :L   FW 254
001A      :T   DW  37
001B      :                                  -------------------------------
001C      :L   RS  60                        SAVE RS DATA
001D      :T   DW  45
001E      :L   RS  61                        REQUIRED ONLY FOR 150U AND
001F      :T   DW  46                        135U WITH PRESET. OF RESTART
0020      :L   RS  62                        MODE IN DX0
0021      :T   DW  47                        (AUTO. WARM RESTART ON
0022      :L   RS  63                        POWER-UP)
0023      :T   DW  48                        SYSTEM DATA RS150 - RS153
0024      :                                  MUST BE SAVED IN 150U
0025      :***                               -------------------------------


NETWORK 3      0026          RESET AUXILIARY FLAGS
0026      :L   KH 0000
0028      :T   FY  60    -NPOS
0029      :T   FY  61    -RESPONSE
002A      :T   FY  62    -CNTL
002B      :T   FY  63    -STATBITS
002C      :T   FY  64    -STATUS
002D      :T   FY  65    -ERROR
002E      :T   FY  66    -FBPOS
002F      :T   FY  67    -EJECTPOS
0030      :T   FW  68    -INTCH1
0031      :***                                -------------------------------
```

```
FY  60   = NPOS                    NO. OF NEXT POS. TO BE APPROACHED
FY  61   = RESPONSE                RESPONSE WHEN POSITION IS REACHED
FY  62   = CNTL                    CONTROL BITS (DL36)
FY  63   = STATBITS                STATUS BITS (DR29)
FY  64   = STATUS                  STATUS FROM POSITIONING PROG. (FB10)
FY  65   = ERROR                   CAUSE OF GROUP ERROR          (F64.7)
FY  66   = FBPOS                   FEEDBACK POSITION NUMBER      (DR28)
FY  67   = EJECTPOS                NEXT EJECT POS. TO BE APPROACHED
FW  68   = INTCH1                  INTERR.REQUEST BYTES CHANNEL 1

NETWORK 4      0032          CONFIGURE IP 240
0032      :JU  FB 167
0033 NAME :STRU.POS
0034 BGAD :    KF +128
0035 KANR :    KF +1
0036 DBNR :    KF +128
0037 AFL  :    KF +1
0038 IMP  :    KF +10
0039 BCD  :    KY 1,1
003A PRA1 :    KM 00000000 00000001
003B PRA2 :    KM 00000000 00011111
003C RUND :    KF +0
003D LOSE :    KF +0
003E DAV  :    KF +1
003F PAFE :    FY 200  -PAFE
0040 BER  :    KF +0                          NOT FOR 115U AND 135U
0041 ABIT :    KY 0,0                          II  II  II  II   II
0042      :
0043      :L   FY 200    -PAFE
0044      :L   KH 0000
0046      :><F
0047      :S   F   65.7  -ERR07
0048      :C   DB 128    -DBCH1
0049      :L   DW  10
004A      :C   DB 100    -DATA1
004B      :T   DW   0    -DW0
004C      :C   DB 128    -DBCH1
004D      :L   DW  13
004E      :C   DB 100    -DATA1
004F      :T   DW   1    -DW1
0050      :***

FY 200   = PAFE                    SEE INSTRUCTION MANUAL SECT. 6.4
F   65.7 = ERR07                   PAFE GROUP ERROR FLAG (-> FY200)
DW   0   = DW0                     RESTART ERR.FLAGGED BY FB167 (DW10)
DW   1   = DW1                     RESTART ERR.FLAGGED BY FB167 (DW13)

DB 128   = DBCH1                   DATA BLOCK CHANNEL 1
DB 100   = DATA1                   TRAVERSING DATA / ERROR FLAGS
```

```
NETWORK 5      0051          RELOAD SCRATCH FLAGS / RS DATA
0051      :                              ----------------------------
0052      :L   DW  30                    RELOAD FLAGS 240-255
0053      :T   FW 240
0054      :L   DW  31                    REQUIRED ONLY AS IN
0055      :T   FW 242                    NETWORK 2 (SAVE SCRATCH
0056      :L   DW  32                    FLAGS / RS DATA)
0057      :T   FW 244
0058      :L   DW  33
0059      :T   FW 246
005A      :L   DW  34
005B      :T   FW 248
005C      :L   DW  35
005D      :T   FW 250
005E      :L   DW  36
005F      :T   FW 252
0060      :L   DW  37
0061      :T   FW 254
0062      :                              ------------------------------
0063      :L   DW  45                    RELOAD RS DATA
0064      :T   RS  60
0065      :L   DW  46                    REQUIRED ONLY AS PER
0066      :T   RS  61                    NETWORK 2 (SAVE SCRATCH FLAGS /
0067      :L   DW  47                              RS DATA)
0068      :T   RS  62                    FOR 150U: RS150 - RS153
0069      :L   DW  48
006A      :T   RS  63
006B      :
006C      :BE
```

```
FB 30

NETWORK 1     0000          READ ACTUAL VALUE FROM IP 240

##############################
#                            #
# CYCLIC PROGRAM FOR X AXIS  #
#                            #
##############################

NAME :X-ACHSE

0005      :C   DB 128    -DBCH1
0006      :
0007      :JU  FB 168                          ------------------------------
0008 NAME :STEU.POS
0009 DBNR :    KF +0
000A FKT  :    KY 1,0                          READ ACT. VAL. AND STATUS AREA
000B PAFE :    FY 200    -PAFE
000C      :L   FY 200    -PAFE
000D      :L   KH 0000
000F      :><F
0010      :S   F   65.7  -ERR07
0011      :
0012      :L   DR  28
0013      :T   FY  66    -FBPOS
0014      :L   DR  29
0015      :T   FY  63    -STATBITS
0016      :
0017      :***

FY 200   = PAFE                    SEE INSTRUCTION MANUAL SECT. 6.4
F   65.7 = ERR07                   PAFE GROUP ERROR FLAG (->FY200)
FY  66   = FBPOS                   FEEDBACK POSITION NUMBER (DR28)
FY  63   = STATBITS                STATUS BITS (DR29)

DB 128   = DBCH1                   DATA BLOCK CHANNEL 1

NETWORK 2      0018          ENABLE / MAIN SWITCH
0018      :A   I   32.0  -MAINSW               --------------------------------
0019      :JC  =NTW3
001A      :A   F    0.0  -RLO0                 RESET PROGRAM
001B      :=   Q    4.0  -POSDIR
001C      :=   Q    4.1  -NEGDIR
001D      :=   Q    4.2  -HOOTER
001E      :=   Q    5.0  -OPENGR
001F      :=   Q    5.1  -CLOSGR
0020      :L   KH 0000
0022      :SD  T    1    -POSTIMER
0023      :SD  T    2    -STOPTIMER
0024      :SD  T    3    -REFTIMER
0025      :T   FY   60   -NPOS
0026      :T   FY   61   -RESPONSE
0027      :T   FY   62   -CNTL
0028      :T   FY   63   -STATBITS
0029      :T   FY   64   -STATUS
002A      :T   FY   65   -ERROR
002B      :T   FY   66   -FBPOS
002C      :T   FY   67   -EJECTPOS
002D      :T   DL   36
002E      :JU  FB  168
002F NAME :STEU.POS
0030 DBNR :    KF +0
0031 FKT  :    KY 20,0                         FORWARD CONTROL BITS TO IP
0032 PAFE :    FY 200    -PAFE
0033      :BEU
0034 NTW3 :***
```

```
I   32.0 = MAINSW                   MAIN SWITCH: ENABLE FOR CONTROL SYSTEM
F    0.0 = RLO0                     FLAG FOR "0" SIGNAL
Q    4.0 = POSDIR                   OUTPUT FOR DIRECTION CONTROL
Q    4.1 = NEGDIR                   OUTPUT FOR DIRECTION CONTROL
Q    4.2 = HOOTER                   ACOUSTIC FAULT SIGNAL
Q    5.0 = OPENGR                   OUTPUT 'OPEN GRIPPER'
Q    5.1 = CLOSGR                   OUTPUT 'CLOSE GRIPPER'
T    1   = POSTIMER                 WATCHDOG TIMER FOR POSITIONING
T    2   = STOPTIMER                TIMER FOR MOTOR DECELERATION
T    3   = REFTIMER                 DELAY FOR ZERO MARK AFTER PRELIM.CONT.
FY  60   = NPOS                     NO. OF NEXT POS. TO BE APPROACHED
FY  61   = RESPONSE                 RESPONSE WHEN POSITION IS REACHED
FY  62   = CNTL                     CONTROL BITS (DL36)
FY  63   = STATBITS                 STATUS BITS  (DR29)
FY  64   = STATUS                   STATUS FROM POSITIONING PROG. (FB10)
FY  65   = ERROR                    CAUSE OF GROUP ERROR FLAG     (F64.7)
FY  66   = FBPOS                    FEEDBACK POSITION NUMBER      (DR28)
FY  67   = EJECTPOS                 NEXT EJECT POS. TO BE APPROACHED
FY 200   = PAFE                     SEE MANUAL SECTION 6.4


NETWORK 3      0035          REFERENCE POINT APPROACH
0035      :                                  ------------------------------
0036      :AN  F   64.3  -REFEND
0037      :JC  FB  31
0038 NAME :REFFAHRT
0039      :
003A      :***

F   64.3 = REFEND                   END OF REFERENCE POINT APPROACH


NETWORK 4      003B          SET UP POSITIONS
003B      :O   F   64.2  -REFACTIV
003C      :O   F   64.0  -POSACTIV
003D      :O   Q    5.0  -OPENGR              RESPONSES COMPLETED
003E      :O   Q    5.1  -CLOSGR
003F      :JC  =NTW5
0040      :                                  ----------------------------
0041      :C   DB 100    -DATA1
0042      :
0043      :A   F   64.5  -MACHCYC
0044      :JC  =AUSW
0045      :A   I   32.1  -START
0046      :JC  =STRT
0047      :L   DR  11    -HOMEPOS            POS.NO. FOR HOME POS.
0048      :T   FY  60    -NPOS
0049      :L   KH 0000                       RESET RESPONSES
004B      :T   FY  61    -RESPONSE
004C      :JU  =NTW5
004D STRT :                                  START MEASURES
004E      :L   DL  11    -MACHPOS            POS.NO. FOR PICKUP POINT
004F      :T   FY  60    -NPOS
0050      :L   DR  12    -DR12               POS.NO. OF 1ST EJECT POS.
0051      :T   FY  67    -EJECTPOS
0052      :A   F    0.1  -RLO1
0053      :S   F   61.1  -RESP02              READY RESPONSE
0054      :R   F   61.0  -RESP01
0055      :S   F   64.5  -MACHCYC             AUXILIARY FLAG
0056      :JU  =NTW5
0057 AUSW :                                  SELECTION OF NEXT POS.
0058      :JU  FB  32                        AND RESPONSE
0059 NAME :AUSWAHL
005A      :
005B NTW5 :***
```

```
F   64.2 = REFACTIV                 REF.POINT APPROACH IN PROGRESS
F   64.0 = POSACTIV                 POSITIONING IN PROGRESS
Q    5.0 = OPENGR                   OPEN GRIPPER OUTPUT
Q    5.1 = CLOSGR                   CLOSE GRIPPER OUTPUT
F   64.5 = MACHCYC                  MACHINING CYCLE IN PROGRESS
I   32.1 = START                    START OF POSITIONING PROGRAM
DR  11   = HOMEPOS                  POS.NO. FOR HOME POSITION
FY  60   = NPOS                     NO. OF NEXT POS. TO BE APPROACHED
FY  61   = RESPONSE                 RESPONSE WHEN POSITION IS REACHED
DL  11   = MACHPOS                  POS. NO. FOR PICKUP POINT
DR  12   = DR12                     FIRST EJECT POSITION
FY  67   = EJECTPOS                 NEXT EJECT POS. TO BE APPROACHED
F    0.1 = RLO1                     FLAG FOR "1" SIGNAL
F   61.1 = RESP02                   CLOSE GRIPPER
F   61.0 = RESP01                   OPEN GRIPPER

DB 100   = DATA1                    TRAVERSING DATA / ERROR FLAGS


NETWORK 5      005C          POSITIONING
005C      :
005D      :AN  F   64.2  -REFACTIV
005E      :AN  Q    5.0  -OPENGR
005F      :AN  Q    5.1  -CLOSGR
0060      :JC  FB  33
0061 NAME :POS/ANW
0062      :
0063      :***

F   64.2 = REFACTIV                 REF. POINT APPROACH IN PROGRESS
Q    5.0 = OPENGR                   OPEN GRIPPER OUTPUT
Q    5.1 = CLOSGR                   CLOSE GRIPPER OUTPUT


NETWORK 6      0064          ERROR / LIMIT SWITCH MONITORING
0064      :                                  ------------------------------
0065      :A   F   64.3  -REFEND
0066      :AN  F   63.0  -SYNC               SYNCHRONIZATION MONITORING
0067      :S   F   65.6  -ERR06
0068      :                                  ------------------------------
0069      :O   F   65.0  -ERR00              GENERATE GROUP ERROR FLAG
006A      :O   F   65.6  -ERR06
006B      :O   F   65.7  -ERR07
006C      :S   F   64.7  -FAULT
006D      :                                  ------------------------------
006E      :O   F   65.0  -ERR00              ERROR FLAGS WHICH RESULT IN
006F      :O   F   65.4  -ERR04              DRIVE SHUTDOWN
0070      :O   F   65.5  -ERR05
0071      :O   F   65.6  -ERR06
0072      :O   F   65.7  -ERR07
0073      :R   Q    4.0  -POSDIR
0074      :R   Q    4.1  -NEGDIR
0075      :                                  ------------------------------
0076      :A   F   64.3  -REFEND             LIMIT SWITCH MONITORING
0077      :AN  I   33.1  -ENDNEG             AXIS
0078      :R   Q    4.1  -NEGDIR
0079      :S   F   64.6  -AUXF01
007A      :
007B      :AN  I   33.0  -ENDPOS
007C      :R   Q    4.0  -POSDIR
007D      :S   F   64.6  -AUXF01
007E      :
007F      :A   I   33.0  -ENDPOS
0080      :A   I   33.1  -ENDNEG
0081      :R   F   64.6  -AUXF01             ------------------------------
```

```
0082      :
0083      :A   I   33.2  -GRUP               LIMIT SWITCH MONITORING
0084      :R   Q    5.1  -CLOSGR             GRIPPER
0085      :
0086      :A   I   33.3  -GRDOWN
0087      :R   Q    5.0  -OPENGR
0088      :S   Q    5.1  -CLOSGR             ------------------------
0089      :
008A      :A   F   64.6  -AUXF01             SECONDS CLOCK PULSE FOR
008B      :AN  T    5    -STOPCLK            ACOUSTIC LIMIT SW. SIGNAL
008C      :L   KT 050.0
008E      :SD  T    4    -STRTCLK
008F      :A   T    4    -STRTCLK
0090      :SD  T    5    -STOPCLK
0091      :                                  -------------------------
0092      :A   T    4    -STRTCLK            LIMIT SWITCH
0093      :O   F   64.7  -FAULT              OTHER FAULT
0094      :=   Q    4.2  -HOOTER             OUTPUT ACOUSTIC SIGNAL
0095      :
0096      :BE

F   64.3 = REFEND                  REFERENCE POINT APPROACH TERMINATED
F   63.0 = SYNC                    STATUS BIT
F   65.6 = ERR06                   ACT.VAL. NO LONGER SYNCHRONIZED
F   65.0 = ERR00                   REF.POINT APPR. TERM. WITHOUT SYNC.
F   65.7 = ERR07                   PAFE GROUP FLAG (-> FY200)
F   64.7 = FAULT                   GROUP FAULT FLAG (-> FLAG BYTE 65)
F   65.4 = ERR04                   PERM. POSITIONING TIME EXCEEDED
F   65.5 = ERR05                   INTERRUPT BITS DRB, NPU, OVF
Q    4.0 = POSDIR                  OUTPUT FOR DIRECTION CONTROL
Q    4.1 = NEGDIR                  OUTPUT FOR DIRECTION CONTROL
I   33.1 = ENDNEG                  LIMIT SWITCH FOR NEG. DIRECTION
F   64.6 = AUXF01                  AUXILIARY/SCRATCH FLAG
I   33.0 = ENDPOS                  LIMIT SWITCH FOR POS. DIRECTION
I   33.2 = GRUP                    GRIPPER IN HOME POSITION (UP)
Q    5.1 = CLOSGR                  CLOSE GRIPPER OUTPUT
I   33.3 = GRDOWN                  GRIPPER IN PICKUP/EJECT POS. (DOWN)
Q    5.0 = OPENGR                  OPEN GRIPPER OUTPUT
T    5   = STOPCLK                 CLOCK PULSE FOR ACOUSTIC LIM.SW.SIGNAL
T    4   = STRTCLK                 CLOCK PULSE FOR ACOUSTIC LIM.SW.SIGNAL
Q    4.2 = HOOTER                  ACOUSTIC FAULT SIGNAL
```

```
FB 31

NETWORK 1      0000

############################
#                          #
# REFERENCE POINT APPROACH #
#                          #
############################

NAME :REFFAHRT

0005      :C   DB 128    -DBCH1
0006      :
0007      :A   F   64.2  -REFACTIV
0008      :JC  =VOR1
0009      :                                  -------------------------
000A      :JU  FB 168                        RESET OUTPUTS
000B NAME :STEU.POS
000C DBNR :    KF +0
000D FKT  :    KY 20,1
000E PAFE :    FY 200    -PAFE
000F      :L   FY 200    -PAFE
0010      :L   KH 0000
0012      :><F
0013      :S   F   65.7  -ERR07
0014      :
0015      :A   F   0.1   -RLO1
0016      :S   F  64.2   -REFACTIV
0017      :R   Q   4.0   -POSDIR
0018      :S   Q   4.1   -NEGDIR
0019      :L   KH 0011                       STATUS BITS FREI & HASY
001B      :T   DL 36
001C      :T   FY 62     -CNTL
001D      :JU  FB 168
001E NAME :STEU.POS
001F DBNR :    KF +0
0020 FKT  :    KY 20,0                     TRANSFER CONTROL BITS
0021 PAFE :    FY 200    -PAFE
0022      :L   FY 200    -PAFE
0023      :L   KH 0000
0025      :><F
0026      :S   F   65.7  -ERR07
0027 VOR1 :
0028      :AN  I   33.1  -ENDNEG
0029      :=   Q    6.0  -INSIGNAL           GENERATE PRELIM.CONTACT
002A      :R   Q    4.1  -NEGDIR
002B      :L   KT 020.1                      2 SEC DELAY
002D      :SS  T    2    -STOPTIMER          LATCHING ON DELAY TIMER
002E      :A   T    2    -STOPTIMER
002F      :S   Q    4.1  -POSDIR
0030      :                                  --------------------------
0031      :
0032      :A   Q    4.0  -POSDIR
0033      :L   KT 040.1                      ON DELAY 4 SEC
0035      :SD  T    3    -REFTIMER
0036      :
0037      :AN  T    3    -REFTIMER
0038      :JC  =ENDE
0039      :                                  -------------------------
003A      :A   F    0.0  -RLO0               RESET TIMER
003B      :SD  T    3    -REFTIMER
003C      :SD  T    2    -STOPTIMER
003D      :
003E      :L   KH 0001                       RESET HASY CONTROL BIT
0040      :T   DL  36
0041      :T   FY  62    -CNTL
```

```
0042      :JU  FB 168
0043 NAME :STEU.POS
0044 DBNR :    KF +0
0045 FKT  :    KY 20,0                          TRANSFER CONTROL BITS
0046 PAFE :    FY 200    -PAFE
0047      :L   FY 200    -PAFE
0048      :L   KH 0000
004A      :><F
004B      :S   F   65.7  -ERR07
004C      :                                     --------------------------------
004D      :L   KH 0000                          RESET FREI CONTROL BIT
004F      :T   DL  36
0050      :T   FY  62    -CNTL
0051      :JU  FB 168
0052 NAME :STEU.POS
0053 DBNR :    KF +0
0054 FKT  :    KY 20,0                          TRANSFER CONTROL BITS
0055 PAFE :    FY 200    -PAFE
0056      :L   FY 200    -PAFE
0057      :L   KH 0000
0059      :><F
005A      :S   F   65.7  -ERR07
005B      :                                     --------------------------------
005C      :JU  FB 168
005D NAME :STEU.POS
005E DBNR :    KF +0
005F FKT  :    KY 1,0                           READ ACTUAL VALUE + STATUS
0060 PAFE :    FY 200    -PAFE
0061      :L   FY 200    -PAFE
0062      :L   KH 0000
0064      :><F
0065      :S   F   65.7  -ERR07
0066      :
0067      :L   DR  29
0068      :T   FY  63    -STATMELD
0069      :                                     --------------------------------
006A      :ON  F   63.0  -SYNC                  STATUS CORRECT FOLLOWING
006B      :ON  F   63.2  -BEE1                  REFERENCE POINT APPROACH ?
006C      :ON  F   63.3  -BEE2
006D      :ON  F   63.4  -BEE3
006E      :S   F   65.0  -ERR00
006F      :                                     --------------------------------
007O      :A   F    0.1  -VKE1                  TERMINATE REF. POINT APPROACH
0071      :S   F   64.3  -REFEND
0072      :R   F   64.2  -REFACTIV
0073      :R   Q    4.0  -POSDIR
0074      :R   Q    4.1  -NEGDIR
0075 ENDE :BE
```

```
F   64.2 = REFACTIV                 REF. POINT APPROACH IN PROGRESS
FY 200   = PAFE                     SEE MANUAL SECTION 6.4
F   65.7 = ERR07                    PAFE GROUP FLAG (-> FY200)
F    0.1 = RLO1                     FLAG FOR "1" SIGNAL
Q    4.0 = POSDIR                   OUTPUT FOR DIRECTION CONTROL
Q    4.1 = NEGDIR                   OUTPUT FOR DIRECTION CONTROL
FY  62   = CNTL                     CONTROL BITS (DL36)
I   33.1 = ENDNEG                   LIMIT SW. FOR NEG. DIRECTION
Q    6.0 = INSIGNAL                 PRELIM.CONT. F.CH.1 (INVERSE I33.1)
T    2   = STOPTIMER                TIMER FOR MOTOR DECELERATION
T    3   = REFTIMER                 DELAY F. ZERO MARK AFTER PREL.CONT.
F    0.0 = RLO0                     FLAG FOR "0" SIGNAL
FY  63   = STATBITS                 STATUS BITS (DR29)
F   63.0 = SYNC                     STATUS BIT
F   63.2/63.3/63.4 = BEE1/BEE2/BEE3 STATUS BIT
F   65.0 = ERR00                    REF. POINT APPR. TERM. WITHOUT SYNC
F   64.3 = REFEND                   REF. POINT APPROACH TERMINATED
DB 128   = DBCH1                    DATA BLOCK CHANNEL 1
```

```
FB 32

NETWORK 1     0000

################################################
#                                              #
# SELECTING THE NEXT POSITION TO BE APPROACHED #
#                                              #
################################################


NAME :AUSWAHL

0005      :A   F   61.0  -RESP01
0006      :JC  =VOR2
0007      :A   F   61.1  -RESP02
0008      :JC  =VOR1
0009      :BEU
000A VOR1 :S   F   61.0  -RESP01
000B      :R   F   61.1  -RESP02
000C      :L   FY  67    -EJECTPOS
000D      :T   FY  60    -NPOS
000E      :L   DL  12    -DL12                LAST EJECT POSITION
000F      :>=F
0010      :R   F  64.5   -MACHCYC
0011      :BEU
0012 VOR2 :R   F   61.0  -RESP01
0013      :S   F   61.1  -RESP02
0014      :L   DL  11    -MACHPOS             PICKUP POINT
0015      :T   FY  60    -NPOS
0016      :L   FY  67    -EJECTPOS
0017      :I        1
0018      :T   FY  67    -EJECTPOS
0019      :BE

F   61.0 = RESP01                  OPEN GRIPPER
F   61.1 = RESP02                  CLOSE GRIPPER
FY  67   = EJECTPOS                NEXT EJECT POS. TO BE APPROACHED
FY  60   = NPOS                    NO. OF NEXT POS. TO BE APPROACHED
DL  12   = DL12                    LAST EJECT POSITION
F   64.5 = MACHCYC                 MACHINING CYCLE IN PROGRESS
DL  11   = MACHPOS                 POS. NO. FOR PICKUP POINT
```

```
FB 33

NETWORK 1     0000

################################################
#                                              #
# TRANSFER POSITION NUMBERS TO IP, POSITIONING #
#                                              #
################################################

NAME :POS/ANW

0005      :C   DB 128    -DBCH1               OPEN IP DATA BLOCK
0006      :A   F   64.0  -POSACTIV
0007      :O
0008      :L   FY  60    -NPOS
0009      :L   FY  66    -FBPOS
000A      :!=F
000B      :JC  =NTW2                          -------------------------
000C      :A   F    0.1  -RLO1
000D      :L   KT 300.1                       MONITORING TIME = 30 SEC
000F      :SD  T    1    -POSTIMER
0010      :S   F   64.0  -POSACTIV            PROGRAM STATUS
0011      :R   F   64.1  -POSREADY
0012      :R   F   65.1  -ERR01
0013      :R   F   65.2  -ERR02
0014      :R   F   65.3  -ERR03
0015      :R   F   65.4  -ERR04
0016      :R   F   64.7  -FAULT               -------------------------
0017      :
0018      :L   KH 0001                        SET CONTROL BIT "FREI"
001A      :T   DL  36
001B      :T   FY  62    -CNTL
001C      :
001D      :L   KY 21,0                        INDIRECT INITIALIZATION
001F      :L   FY  60    -NPOS                OF FUNCTION "WRITE
0020      :OW                                 CONTROL BITS AND POS.NO."
0021      :T   DW  19
0022      :JU  FB 168
0023 NAME :STEU.POS
0024 DBNR :    KF +0
0025 FKT  :    KY 0,0                         INDIRECT INITIALIZATION
0026 PAFE :    FY 200   -PAFE                 OVER DATA WORD 19
0027      :L   FY 200   -PAFE
0028      :L   KH 0000
002A      :><F
002B      :S   F   65.7  -ERR07               -------------------------
002C      :
002D      :JU  FB 168
002E NAME :STEU.POS
002F DBNR :    KF +0
0030 FKT  :    KY 1,0                         READ ACT.VAL.+STATUS AREA
0031 PAFE :    FY 200   -PAFE
0032      :L   FY 200   -PAFE
0033      :L   KH 0000
0035      :><F
0036      :S   F   65.7  -ERR07               -------------------------
0037      :
0038      :L   DR  28                         TRANSFER STATUS INFO
0039      :T   FY  66    -FBPOS               TO FLAGS
003A      :L   DR  29
003B      :T   FY  63    -STATBITS
003C      :                                   -------------------------
003D      :A   F   63.3  -BEE2                SELECT DIRECTION, THUS
003E      :AN  F   63.1  -RICH                ENABLING DRIVE
003F      :=   Q    4.0  -POSDIR
0040      :JC  =NTW2
```

```
0041      :
0042      :A   F   63.3  -BEE2
0043      :A   F   63.1  -RICH
0044      :=   Q    4.1  -NEGPOS
0045      :JC  =NTW2                          -------------------------
0046      :
0047      :A   F    0.0  -RLO0
0048      :SD  T    1    -POSTIMER            STOP TIMER
0049      :SD  T    2    -STOPTIMER
004A      :=   F   64.0  -POSACTIV            PROGRAM STATUS
004B      :                                   -------------------------
004C      :A   F   63.4  -BEE3                WHEN ACT.VAL. BETWEEN
004D      :S   F   64.7  -FAULT               CUT-OFF & TARGET RANGE
004E      :S   F   65.1  -ERR01
004F      :JC  =NTW2                          -------------------------
0050      :
0051      :AN  F   64.1  -POSREADY            MESSAGE
0052      :S   F   64.1  -POSREADY
0053      :
0054      :A   F   61.0  -RESP01              INITIATE REACTION
0055      :AN  F   61.1  -RESP02
0056      :S   Q    5.0  -OPENGR
0057      :A   F   61.1  -RESP02
0058      :AN  F   61.0  -RESP01
0059      :S   Q    5.1  -CLOSGR
005A      :                                   -------------------------
005B NTW2 :
005C      :A   F   64.1  -POSREADY            PROGRAM STATUS
005D      :R   F   64.0  -POSACTIV
005E      :R   Q    4.0  -POSDIR              RESET OUTPUTS
005F      :R   Q    4.1  -NEGDIR
0060      :***

F   64.0 = POSACTIV                POSITIONING IN PROGRESS
FY  60   = NPOS                    NO. OF NEXT POS. TO BE APPROACHED
FY  66   = FBPOS                   FEEDBACK POS. NO. (DR28)
F    0.1 = RLO1                    FLAG FOR "1" SIGNAL
T    1   = POSTIMER                WATCHDOG TIMER F. POSITIONING
F   64.1 = POSREADY                POS. REACHED, RESPONSES INITIATED
F   65.1 = ERR01                   DIST.ACT.POS. TO SETP.POS.TOO SMALL
F   65.2 = ERR02                   TARGET RANGE NOT REACHED
F   65.3 = ERR03                   TARGET RANGE EXITED (ZBV)
F   65.4 = ERR04                   PERM. TIME F. POSITIONING EXCEEDED
F   64.7 = FAULT                   GROUP FAULT (-> FLAG BYTE 65)
FY  62   = CNTL                    CONTROL BITS (DL36)
FY 200   = PAFE                    SEE MANUAL SECTION 6.4
F   65.7 = ERR07                   PAFE GROUP ERR.FLAG (-> FY200)
FY  63   = STATBITS                STATUS BITS (DR29)
F   63.3 = BEE2                    STATUS BIT
F   63.1 = RICH                    STATUS BIT
Q    4.0 = POSDIR                  OUTPUT FOR DIRECTION CONTROL
Q    4.1 = NEGDIR                  OUTPUT FOR DIRECTION CONTROL
F    0.0 = RLO0                    FLAG FOR "0" SIGNAL
T    2   = STOPTIMER               TIMER FOR MOTOR DECELERATION
F   63.4 = BEE3                    STATUS BIT
F   61.0 = RESP01                  OPEN GRIPPER
F   61.1 = RESP02                  CLOSE GRIPPER
Q    5.0 = OPENGR                  OPEN GRIPPER OUTPUT
Q    5.1 = CLOSGR                  CLOSE GRIPPER OUTPUT

DB 128   = DBCH1                   DATA BLOCK CHANNEL 1
```

```
NETWORK 2      0061          ERROR MONITORING
0061      :A   T    1    -POSTIMER            WHEN TIME EXCEEDED
0062      :S   F   65.4  -ERR04
0063      :S   F   64.7  -FAULT
0064      :
0065      :A   T    2    -STOPTIMER           WHEN TIMER RAN DOWN
0066      :S   F   65.2  -ERR02               BEF. INT.BIT BE3 WAS SET
0067      :S   F   64.7  -FAULT
0068      :
0069      :BE

T    1   = POSTIMER                WATCHDOG TIMER FOR POSITIONING
F   65.4 = ERR04                   PERM.TIME FOR POSITIONING EXCEEDED
F   64.7 = FAULT                   GROUP FAULT FLAG (-> FLAG BYTE 65)
T    2   = STOPTIMER               TIMER FOR MOTOR DECELERATION
F   65.2 = ERR02                   TARGET RANGE NOT REACHED
```

```
FB 34

NETWORK 1      0000

########################################
# INTERRUPT SERVICE ROUTINE FOR X AXIS #
#                                      #
########################################

NAME :ALARM/K1

0005      :C   DB 100    -DATA1               -------------------------
0006      :L   FW 240                         SAVE SCRATCH FLAGS
0007      :T   DW  20
0008      :L   FW 242                         REQUIRED ONLY FOR 115U,
0009      :T   DW  21                         155U (IN 155U MODE) AND
000A      :L   FW 244                         135U WHEN SET IN DX0 FOR
000B      :T   DW  22                         "INTERRUPT SERVICING
000C      :L   FW 246                          AFTER EVERY STATEMENT"
000D      :T   DW  23
000E      :L   FW 248
000F      :T   DW  24
0010      :L   FW 250
0011      :T   DW  25
0012      :L   FW 252
0013      :T   DW  26
0014      :L   FW 254
0015      :T   DW  27
0016      :                                   -------------------------
0017      :L   RS  60                         SAVE SYSTEM DATA
0018      :T   DW  40
0019      :L   RS  61                         REQUIRED ONLY FOR 155U
001A      :T   DW  41                         (IN 155 MODE) AND 135U
001B      :L   RS  62                         WHEN SET IN DX0 FOR:
001C      :T   DW  42                         "INTERRUPT SERVICING
001D      :L   RS  63                          AFTER EVERY STATEMENT"
001E      :T   DW  43                         -------------------------
001F      :
0020      :***


DB 100   = DATA1                   TRAVERSING DATA / ERROR CODES

NETWORK 2      0021          READ INTERRUPT REQUEST BYTES
0021      :
0022      :JU  FB   168
0023 NAME :STEU.POS
0024 DBNR :    KF +128
0025 FKT  :    KY 3,0
0026 PAFE :    FY 201
0027      :L   FY 201
0028      :L   KH 0000
002A      :><F
002B      :S   F   65.7  -ERR07
002C      :
002D      :C   DB 128    -DBCH1
002E      :L   DW  20
002F      :T   FW  68    -INTCH1
0030      :***

F   65.7 = ERR07                   PAFE GROUP FLAG (-> FY200)
FW  68   = INTCH1                  INTERRUPT REQUEST BYTES CHANNEL 1


DB 128   = DBCH1                   DATA BLOCK CHANNEL 1
```

```
NETWORK 3      0031          CUT-OFF RANGE REACHED
0031      :AN  F   69.3  -BE2
0032      :JC  =NTW3
0033      :A   F    0.1  -RLO1
0034      :L   KT 100.0                      START WATCHDOG TIMER (1 SEC)
0036      :SD  T    2    -STOPTIMER
0037 NTW3 :***

F   69.3 = BE2                      IR BEE2 ENTERED
F    0.1 = RLO1                     FLAG FOR "1" SIGNAL
T    2   = STOPTIMER                TIMER FOR MOTOR DECELERATION


NETWORK 4      0038          POSITION REACHED
0038      :AN  F   69.4  -BE3
0039      :JC  =NTW4
003A      :L   KH 0000
003C      :A   F    0.0  -RLO0              STOP TIMER
003D      :SD  T    1    -POSTIMER
003E      :SD  T    2    -STOPTIMER
003F      :
0040      :A   F   61.0  -RESP01            INITIATE RESPONSES
0041      :AN  F   61.1  -RESP02
0042      :S   Q    5.0  -OPENGR
0043      :A   F   61.1  -RESP02
0044      :AN  F   61.0  -RESP01
0045      :S   Q    5.1  -CLOSGR
0046      :
0047      :AN  F   64.1  -POSREADY
0048      :S   F   64.1  -POSREADY
0049 NTW4 :***

F   69.4 = BE3                      IR BEE3 ENTERED
F    0.0 = RLO0                     FLAG FOR "0" SIGNAL
T    1   = POSTIMER                WATCHDOG TIMER FOR POSITIONING
T    2   = STOPTIMER                TIMER FOR MOTOR DECELERATION
F   61.0 = RESP01                   OPEN GRIPPER
F   61.1 = RESP02                   CLOSE GRIPPER
Q    5.0 = OPENGR                   OPEN GRIPPER OUTPUT
Q    5.1 = CLOSGR                   CLOSE GRIPPER OUTPUT
F   64.1 = POSREADY                 POSITION REACHED, RESPONSES INITIATED


NETWORK 5      004A          POSITION ERROR
004A      :AN  F   68.4  -ZBV
004B      :JC  =NTW5
004C      :S   F   65.3  -ERR03
004D      :S   F   64.7  -FAULT
004E      :R   Q    4.0  -POSDIR
004F      :R   Q    4.1  -NEGDIR
0050 NTW5 :***

F   68.4 = ZBV                      IR TARGET RANGE (BEE3) EXITED
F   65.3 = ERR03                    TARGET RANGE EXITED (ZBV)
F   64.7 = FAULT                    GROUP FAULT FLAG (-> FLAG BYTE 65)
Q    4.0 = POSDIR                   OUTPUT FOR DIRECTION
Q    4.1 = NEGDIR                   OUTPUT FOR DIRECTION
```

```
NETWORK 6      0051          HARDWARE FAULTS
0051      :AN  F   68.0  -UEB
0052      :AN  F   68.1  -NPU
0053      :AN  F   68.2  -DRB
0054      :JC  =NTW6
0055      :S   F   65.5  -ERR05
0056      :S   F   64.7  -FAULT
0057      :R   Q    4.0  -POSDIR
0058      :R   Q    4.1  -NEGDIR
0059 NTW6 :***


F   68.0 = UEB                      IR COUNT IN OVERRANGE
F   68.1 = NPU                      IR ZERO MARK ERROR
F   68.2 = DRB                      IR WIREBREAK/SHORT-CIRCUIT
F   65.5 = ERR05                    INTERRUPTS DRB, NPU, OVF
F   64.7 = FAULT                    GROUP FAULT FLAG (-> FLAG BYTE 65)
Q    4.0 = POSDIR                   OUTPUT FOR DIRECTION
Q    4.1 = NEGDIR                   OUTPUT FOR DIRECTION

NETWORK 7      005A           OUTPUTS
005A      :L   QB   4                        UPDATE OUTPUTS
005B      :T   PY   4
005C      :L   QB   5
005D      :T   PY   5
005E      :***


NETWORK 8      005F          RELOAD SCRATCH FLAG/SYSTEM DATA
005F      :C   DB 100    -DATA1               ------------------------
0060      :L   DW  20                         RELOAD SCRATCH FLAGS
0061      :T   FW 240
0062      :L   DW  21
0063      :T   FW 242
0064      :L   DW  22
0065      :T   FW 244
0066      :L   DW  23
0067      :T   FW 246
0068      :L   DW  24
0069      :T   FW 248
006A      :L   DW  25
006B      :T   FW 250
006C      :L   DW  26
006D      :T   FW 252
006E      :L   DW  27
006F      :T   FW 254
0070      :                                   -------------------------
0071      :L   DW  40                         RELOAD SYSTEM DATA
0072      :T   RS  60
0073      :L   DW  41                         SAME LOGIC AS IN
0074      :T   RS  61                         NETWORK 1
0075      :L   DW  42
0076      :T   RS  62
0077      :L   DW  43
0078      :T   RS  63
0079      :
007A      :BE


DB 100   = DATA1                    TRAVERSING DATA/ERROR CODES
```

```
FB 167

NETWORK 1      0000
NAME :STRU.POS
ID   :BGAD      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :KANR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DBNR      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :AFL       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :IMP       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :BCD       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KY
ID   :PRA1      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KM
ID   :PRA2      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KM
ID   :RUND      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :LOSE      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :DAV       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :PAFE      I/Q/D/B/T/C: Q  BI/BY/W/D: BY
ID   :BER       I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :ABIT      I/Q/D/B/T/C: D  KM/KH/KY/KS/KF/KT/KC/KG: KY

002F      :BE


FB 168

NETWORK 1      0000
NAME :STEU.POS
ID   :DBNR      I/Q/D/B/T/C: D KM/KH/KY/KS/KF/KT/KC/KG: KF
ID   :FKT       I/Q/D/B/T/C: D KM/KH/KY/KS/KF/KT/KC/KG: KY
ID   :PAFE      I/Q/D/B/T/C: Q BI/BY/W/D: BY

000E      :BE



OB 1

NETWORK 1     0000

##############################################
#                                            #
# ORGANIZATION BLOCK FOR THE CYCLIC PROGRAM #
#                                            #
##############################################

0000      :
0001      :JU  FB  30
0002 NAME :X-ACHSE
0003      :
0004      :
0005      :BE
```

```
OB 2

NETWORK 1      0000          INTERRUPT SERVICE ROUTINE AXIS 1

################################################
#                                              #
# ORGANIZATION BLOCK FOR INTERRUPT SERVICING #
#                                              #
################################################


0000      :
0001      :
0002      :JU  FB  34
0003 NAME :ALARM/K1
0004      :
0005      :BE


OB 20

NETWORK 1      0000

################################################
#                                              #
# ORGANIZATION BLOCK FOR MANUAL COLD RESTART #
#                                              #
################################################



FOR THE 115U => O B 2 1
                -------


0000      :
0001      :JU  FB  20                          CONFIGURING THE IP 240
0002 NAME :ANLAUF
0003      :
0004      :BE



OB 22

NETWORK 1      0000

#########################################################
#                                                       #
# ORGANIZATION BLOCK FOR AUTOMATIC COLD/WARM RESTART #
#                                                       #
#########################################################


0000      :
0001      :JU  FB  20                          CONFIGURING THE IP 240
0002 NAME :ANLAUF
0003      :
0004      :BE
```

Figures

Tables

11 Direct Data Interchange with the IP 240

For time-critical applications, it may be necessary to exchange data directly with the IP 240 without using the control FBs. This section provides information on

- data interchange with the IP 240.
- the job numbers you must specify so that
  - the IP will provide the data you need,
  - the IP will accept new data.
- the contents of the transfer buffer on the IP 240 in position decoding and counting mode.
  The contents of the transfer buffer for positioning mode are discussed in Chapter 10. In IP 252 expansion mode (S5-115U only), the two IPs interchange data autonomously following configuring, making an interchange between the S5 CPU and the IP 240 unnecessary.

A 16-byte address space is provided for data interchange with the IP 240. The absolute addresses of the individual bytes are a composite of the module start address and an offset of between 0 and 15.

Absolute address=module start address+offset

The address space is subdivided as follows:

Offset 0 to14	Offset 15
With offsets 0 to 14 you address the individual bytes in the transfer buffer. The S5 CPU can read from and write to this buffer.	With offset 15 you address: • the status register, which can be read by the S5 CPU and provides information on the servicing job requests on the IP 240. • the job request register, to which the S5 CPU has write access, to specify the job number.

S5 CPU and IP 240 both have bidirectional data interchange capabilities. The following functional sequences must be observed:

S5 CPU IP 240 Write new, modified data to the IP 240	S5 CPU IP 240 Read current data from the IP 240
To issue a Write request, you must first enter the new data in the transfer buffer, then specify a job number which tells the IP 240 to fetch the data.	To issue a Read request, you must specify a job number indicating which data are to be read. The IP 240 then makes this data available in the transfer buffer, and you can read it out from there.

Note

In order to prevent excessive variations in the IP 240's response time, the IP 240 firmware permits only one data interchange per firmware cycle.
Once new data has been transferred to the IP 240, no further interchanging of data is permitted in the next firmware cycle.

In the following, it has been assumed that the channel has been configured with standard FB 167 for positioning mode, with FB 169 for position decoding mode, or with FB 171 for counting mode.

11.1 Status and Job Request Register (Offset 15)

The IP 240's status register can be read out and its job request register written to under this absolute address (module start address+15).

11.1.1 Status Register

The status register provides information about the status of job order processing on the IP 240 as well as information on channel configuration.

Contents of the status register:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP252	IDLE2	IDLE1	ERR	-	DFRT	AERK	AFRT

Each time you address the transfer buffer (offset 0 to 14), you must first read the status register. Evaluate the bits in this register as follows:

1) The IDLE bit:
   The IP 240 sets this bit to ”0” when the channel was correctly configured.
   If this bit is set, you must first call the relevant configuring FB.

2) The ERR bit:
   The IP 240 sets this bit to ”1” when an error has been flagged on the IP 240.
   You must read and analyze the error code. The last attempted data interchange must be retried with correct values.
   Once the error code has been read, the ERR bit is reset on the IP 240.

3) The AFRT bit:
   The IP 240 sets this bit to ”1” when the last communication cycle was completed without error (this bit is ”1” following configuring with the standard FBs).
   If a data interchange is aborted and the DFRT bit is set, communication with the IP 240 must be reset prior to the start of a new Write or Read cycle. To do so, you must enter 40_H in the IP's job request register.

4) The DFRT bit:
   The IP 240 sets this bit to ”1”,
   - when the required data were made available in the transfer buffer during a Read cycle and can be read out by the S5 CPU or
   - when the data entered in the transfer buffer by the S5 CPU during a Write cycle was fetched.

Table 11-1. Contents of the Status Register

Bit	Abbr.	Meaning when bit is "1"
0	AFRT	Job terminated, The job request was serviced without error.
1	AERK	Job request acknowledged, The IP 240 acknowledged recogniton of a job request (can be evaluated following RESET only).
2	DFRT	Data ready, The data requested was entered in or fetched from the transfer buffer.
4	ERR	**ERR**or, An error has been flagged on the IP 240 and must be read out and analyzed.
5	IDLE1	**IDLE** state, Channel 1 not configured.
6	IDLE2	**IDLE** state, Channel 2 not configured.
7	IP252	**IP 252** expansion, Both channels configured for IP 252 expansion mode.

Note

In Sections 11.2 and 11.3 you will find detailed information on interchanging data with the IP 240. Failure to observe the rules and conventions presented in these sections (e.g. no wait for the relevant bit in the status register) may result in errors both in the data transfer currently in progress as well as in the next exchange of data with the IP.

11.1.2 Job Request Register

The S5 CPU enters the job number in the job request register, thus telling the IP 240 which job it is to execute.

Table 11-2. Contents of the Job Request Register

Job number Chan. 1	Job number Chan. 2	Functional description for mode Position decoding	Counting	Positioning
01_H		Read error codes		
31_H		Read interrupt request bytes for both channels		
40_H		Reset communication with the IP 240 or terminate following serving of a Read request		Reset or terminate communication with the IP 240
10_H	20_H			Write new values for position 1 to 254
11_H	21_H	Write initial and final track values for track 1	Write initial count	Write new values for position 1 to 254
12_H	22_H	Write initial and final track values for track 2		
13 to 16_H	23 to 26_H	Values for track 3 to 6		
17_H	27_H	Write initial and final track values for track 7		
18_H	28_H	Write initial and final track values for track 8		Write new position data for position 0
19_H	29_H	Write zero offset		Write zero offset
$1A_H$	$2A_H$	Write control bits	Write control bits	Write control bits and position number 1 to 254
$1B_H$	$2B_H$	Read actual value and status area	Read actual value, final value and status area	Read actual value, final value and status area
$1D_H$	$2D_H$	Terminate data inter-change after a Write cycle	Terminate data inter-change after a Write cycle	

Note

The job numbers listed in the table are only a few of all possible job numbers. The specification of job numbers not included in the above list is **not permitted**.

11.2 Data Transfer from the IP 240 to the S5 CPU

The S5 CPU can request data from the IP 240. To make this possible, you must enter the appropriate job number in the IP's job request register. The IP 240 sets the DFRT bit in the status register when the requested data are available in the transfer buffer.
In order to prevent errors in a data interchange between IP 240 and S5 CPU, interrupt processing must be disabled while the data interchange is in progress.

The block diagram below shows the communications procedure for ”Read data from the IP 240”.

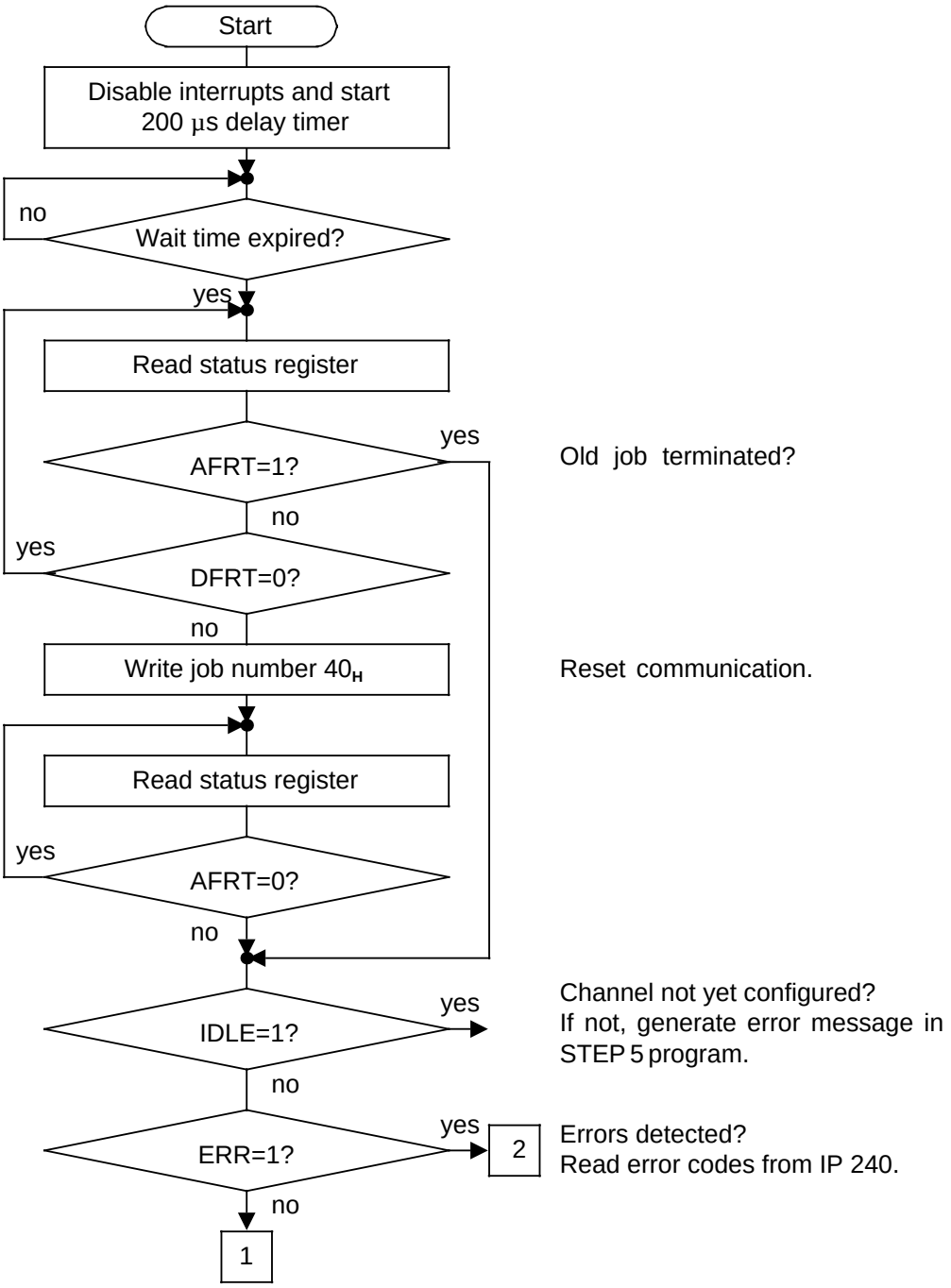


Fig. 11-1. Flowchart for ”Read Data from the IP 240”

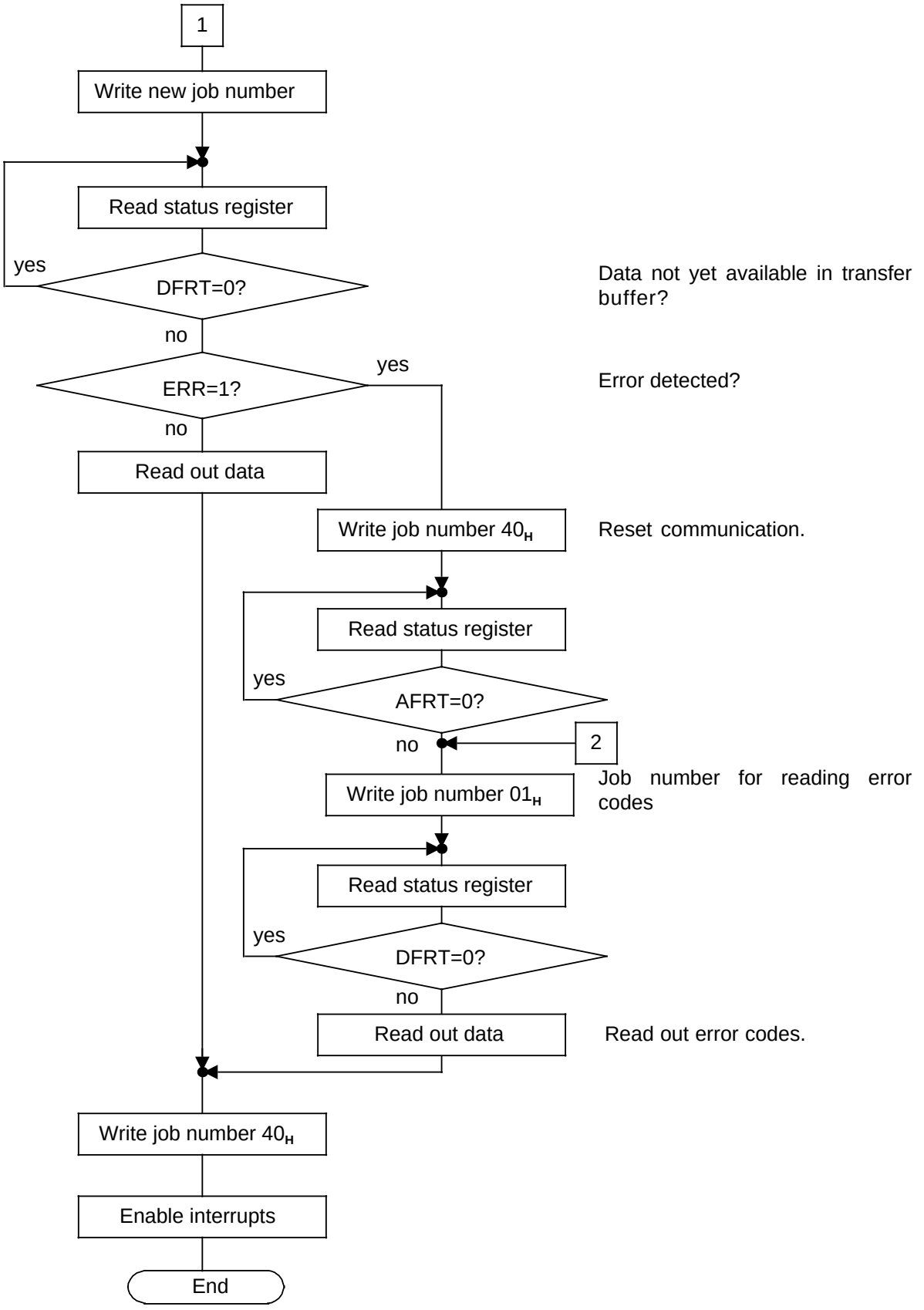


Fig. 11-1. Flowchart for ”Read Data from the IP 240” (Continued)

11.3 Data Transfer from the S5 CPU to the IP 240

The S5 CPU can forward new data to the IP 240. To do so, you must first transfer the new data, then you must enter the appropriate job numbers in the IP's job request register. The IP 240 sets the DFRT bit in the status register when it has fetched this data from the transfer buffer.
To avoid errors during a data interchange between IP 240 and S5 CPU, interrupt servicing must be disabled during data interchange.

"Write data to the IP 240"
You must make preparations for "writing data" to the IP 240 by forwarding a byte, in which you have entered the appropriate job number and set the high-order bit, to the job request register. You can then write the data to the transfer buffer, then tell the IP to fetch this new data by transferring the job number.
In position decoding mode and in counting mode, you terminate this communication cycle by entering $1D_H$ for channel 1 and $2D_H$ for channel 2 in the job request register.
Terminate the communication cycle in positioning mode with 40_H for channel 1 and for channel 2.

Warning

When using direct data interchange in position decoding or counting mode, you must make sure that only valid data are forwarded to the IP 240, as the firmware does not verify this data. During data transfer, data verification is normally taken care of by standard FBs 170 and 172.

Simultaneous transfer of modified track data in position decoding mode
If you want the track data for several modified tracks to become effective simultaneously, proceed as follows:

Transfer the first data batch with the appropriate job number to the IP 240.

Before data interchange is terminated with $1D_H/2D_H$,
enter 40_H in the job request register. As a result, the IP 240 sets the AFRT bit to "1" for the new cycle.
transfer the next batch of data with the appropriate job number to the IP 240.
Repeat for all data to be transferred (Fig. 11.2).

As soon as you have finished data transfer, terminate data interchange with $1D_H$ for channel 1 or $2D_H$ for channel 2.
the modified track data become effective simultaneously .

Note

Once data has been forwarded to the transfer buffer, it is retained until it is overwritten. In order to prevent unintentional reevaluation of old data, you must always overwrite the entire buffer with new data.

The flowchart shown below illustrates the communication procedure for ”Write data to the IP 240”

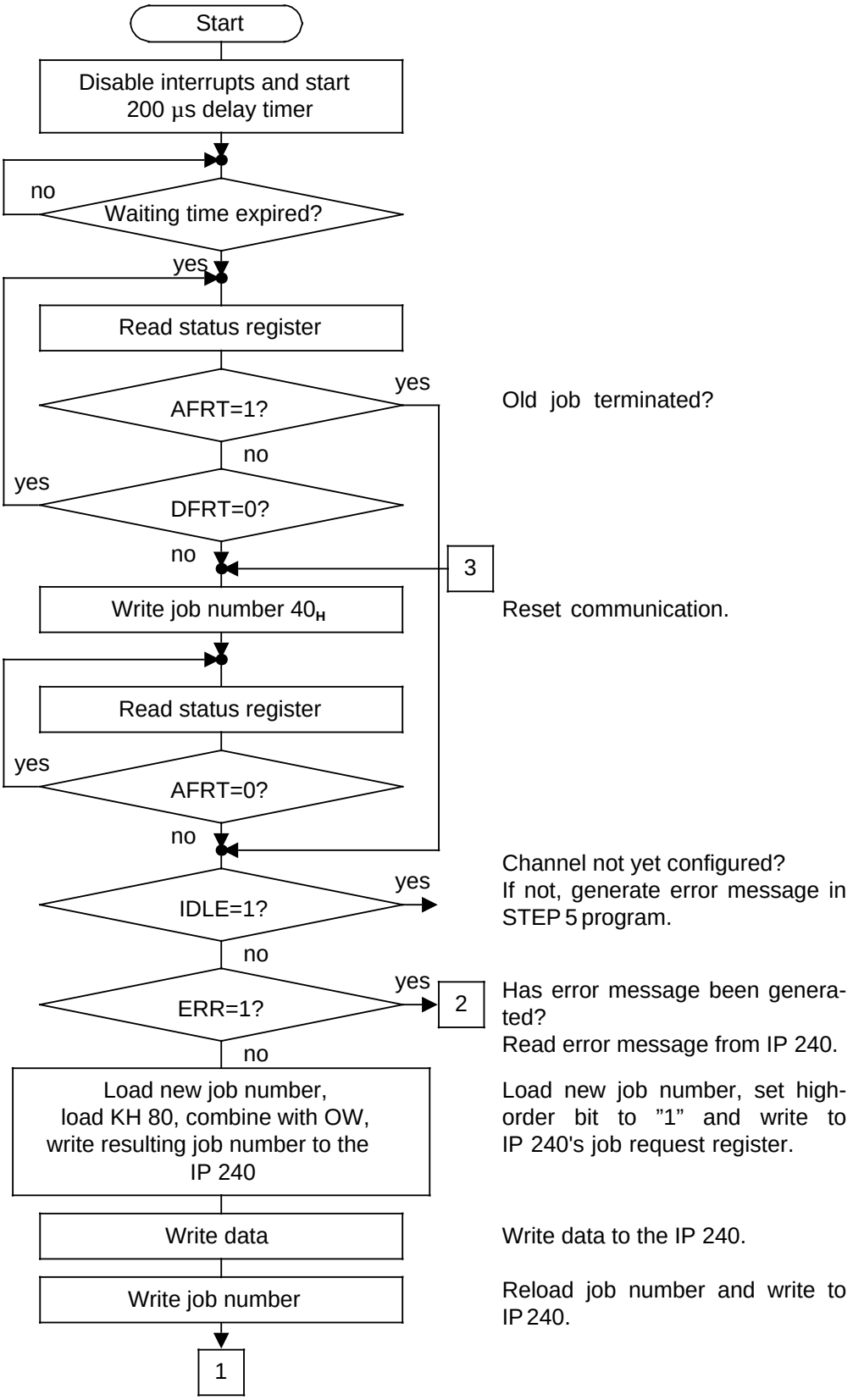


Fig. 11-2. Flowchart for ”Write Data to the IP 240”

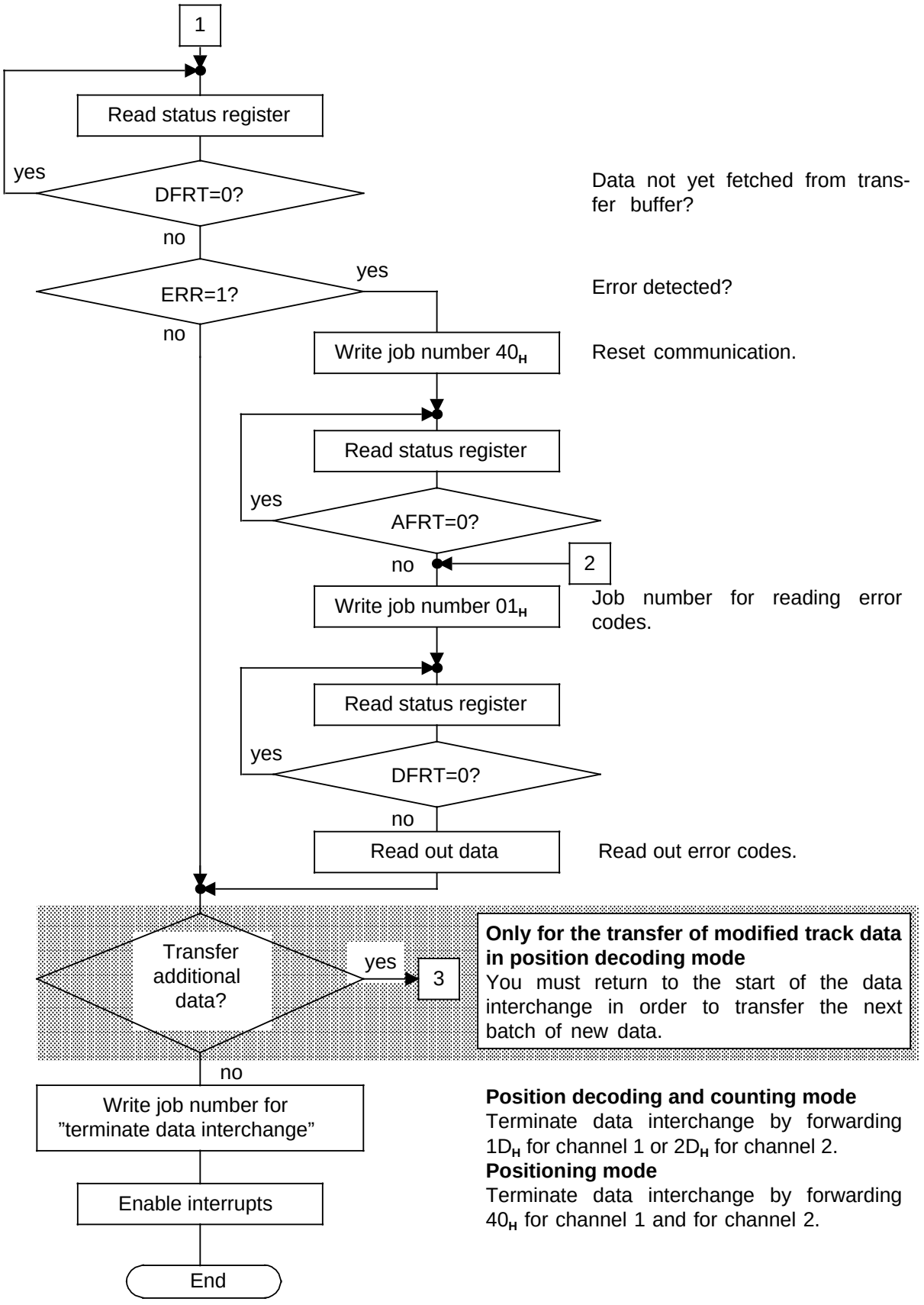


Fig. 11-2. Flowchart for ”Write Data to the IP 240” (Continued)

11.4 Contents of the Transfer Buffer

11.4.1 Position Decoding Mode

Read actual value and status area
When you have transferred job number $1B_H$ (channel 1) or $2B_H$ (channel 2) to the IP 240's job request register, the IP 240 makes the actual value and the status area available in the transfer buffer.

Table 11-3. Contents of the Transfer Buffer on Reading the Actual Value and Status Area, Position Decoding Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	10^1						10^0		Actual value in BCD
1	10^3						10^2		
2	0						10^4		
3	0	. . .		0	0	. . .		0	
4	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Actual value in binary
5	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	
6	0	0	0	0	0	0	0	2^{16}	
7	0	. . .		0	0	. . .		0	Status bit for the actual value
8	0	0	0	0	0	0	UEBL	SG	
9	0	. . .		0	0	. . .		0	
10	0	. . .		0	0	. . .		0	
11	0	. . .		0	0	. . .		0	
12	REF8	REF7	REF6	REF5	REF4	REF3	REF2	REF1	Status bits
13	0	0	0	0	SYNC	0	DRBR	NPUE	
14	DA2	DA1	0	0	0	0	0	0	

Description of the status bits
DA2 =1 Digital output D2 is set
=0 Digital output D2 is not set

DA1 =1 Digital output D1 is set
=0 Digital output D1 is not set

SYNC =1 Reference point approach was terminated with synchronization

DRBR =1 Wirebreak/short-circuit in lines for encoder for symmetrical pulse trains

NPUE =1 Change in number of pulses between two zero mark signals

REFn =1 Actual value lies within track n (including track limits)
=0 Actual value not within track n

UEBL =1 Actual value out of range
(<- 99,999 or>99,999)

SG =1 Actual value is negative
=0 Actual value is positive

Read interrupt request bytes
The IP 240 makes the interrupt request bytes for both channels available when you transfer job number 31_H to the IP 240's job request register.

Table 11-4. Contents of the Transfer Buffer on Reading Interrupt Request Bytes, Position Decoding Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	0	0	0	0	0	DRB	NPU	UEB	Interrupt request bytes for channel 1
1	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	
2	0	0	0	0	0	DRB	NPU	UEB	Interrupt request bytes for channel 2
3	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	
4 to 14	0	. . .		0	0	. . .		0	

Description of the interrupt bits
RFn =1 The interrupt was triggered when the relevant reference bit REFn went to ”1”

DRB =1 The interrupt was triggered by the line monitor

NPU =1 The interrupt was triggered by the zero mark monitor

UEB =1 The interrupt was triggered by an overflow

Note

To prevent the interrupt service OB from being invoked twice when using an S5-150U or S5-155U (150U mode), you must reset the relevant bit in system data 0 immediately after reading the interrupt request bytes. For this the FB 42 is available to you.

Write initial and final track values

To change the initial value and final value for a track, you must load these two values into the transfer buffer and then load the job request register with either $1n_H$ or $2n_H$ (where n=number of the track).

Table 11-5. Contents of the Transfer Buffer on Writing Initial and Final Track Values, Position Decoding Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	10^1						10^0		Initial track value
1	10^3						10^2		
2	0						10^4		
3	0	0	0	0	0	0	0	SG	Sign for initial value SG=1 The initial value is negative. SG=0 The initial value is positive.
4	10^1						10^0		Final track value
5	10^3						10^2		
6	0						10^4		
7	0	0	0	0	0	0	0	SG	Sign for the final value SG=1 The final value is negative. SG=0 The final value is positive.
8 to 14	0	. . .		0	0	. . .		0	

Write zero offset

To specify a zero offset (NVER), you must enter the zero offset value in the transfer buffer and load the job request register with 19_H or 29_H.

Table 11-6. Contents of the Transfer Buffer on Writing a Zero Offset, Position Decoding Mode

Offset tranfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	10^1						10^0		Zero offset
1	10^3						10^2		
2	0						10^4		
3	0	0	0	0	0	0	0	SG	Sign of the NVER SG=1 The zero offset is negative. SG=0 The zero offset is positive.
4 to 14	0	. . .		0	0	. . .		0	

Write control bits

To initialize control bits, you must load the new control bits into the transfer buffer and write job number $1A_H$ or $2A_H$ to the job request register.

Table 11-7. Contents of the Transfer Buffer on Writing Control Bits, Position Decoding Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	0	0	0	0	0	0	0	REFF	Control bits
1	AMSK	0	0	0	DA2F	DA2S	DA1F	DA1S	
2 to14	0	. . .		0	0	. . .		0	

Description of the control bits

AMSK = 1 All interrupts for the channel are masked, i.e. are lost
= 0 Enable interrupts

DA2F	DA2S	
0	0	Digital output D2 is reset
0	1	Digital output D2 is set in accordance with the mode
1	1	Digital output D2 is set irrespective of the actual value

DA1F	DA1S	
0	0	Digital output D1 is reset
0	1	Digital output D1 is set in accordance with the mode
1	1	Digital output D1 is set irrespective of the actual value

REFF = 1 Enable for reference point approach
= 0 Normal actual value acquisition

11.4.2 Counting Mode

Read actual value, final value and status area
The IP 240 makes the actual value, the final value and the status area available in the transfer buffer when you transfer job number $1B_H$ (channel 1) or $2B_H$ (channel 2) to the job request register.

Table 11-8. Contents of the Transfer Buffer on Reading Actual Value, Final Value and Status Area , Counting Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	10^1						10^0		Actual value in BCD
1	10^3						10^2		
2	0	. . .		0	0	. . .		0	
3	0	. . .		0	0	. . .		0	
4	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Actual value in binary
5	0	0	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	
6	0	0	0	0	0	0	0	0	
7	0	. . .		0	0	. . .		0	Status bits for actual value
8	0	0	0	0	0	0	UEBL	SG	SG=1 The actual value is negative SG=0 The actual value is positive
9	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Final value of the last count
10	0	0	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	
11	0	0	0	0	0	UEBS	UEBE	SGF	Status bits for final value
12	0	0	0	0	0	0	REF2	REF1	Status bits
13	0	0	AKTV	TRIG	0	0	0	0	
14	0	DA1	0	0	0	0	0	0	

Description of the status bits

DA1 =1 Digital output D1 is set
=0 Digital output D1 is not set

AKTV =1 Counting was enabled
=0 Counting was not enabled

TRIG =1 Counting has begun (first counting pulse acquired)

REF1 =1 Actual value has reached ”0”
=0 Actual value is not yet ”0”

REF2 =1 Final value was stored

UEBL =1 Actual value out of range (<- 9,999)

UEBE =1 Final value out of range (<- 9,999)

UEBS = 1 Final value overwritten without being read

SG =1 Actual value is negative
=0 Actual value is positive

SGF =1 Final value is negative
=0 Final value is positive

Read interrupt request bytes
The IP 240 makes the interrupt request bytes for both channels available in the transfer buffer when you transfer job number 31_H to the job request register.

Table 11-9. Contents of the Transfer Buffer on Reading Interrupt Request Bytes, Counting Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	0	0	0	0	0	UBS	0	UEB	Interrupt request bytes for channel 1
1	0	0	0	0	0	0	RF2	RF1	
2	0	0	0	0	0	UBS	0	UEB	Interrupt request bytes for channel 2
3	0	0	0	0	0	0	RF2	RF1	
4 to 14	0	. . .		0	0	. . .		0	

Description of the interrupt bits
RF1 =1 The interrupt was triggered because bit REF1 went to ”1”

RF2 =1 The interrupt was triggered because bit REF2 went to ”1”

UEB =1 The interrupt was triggered by a counter overflow

UBS =1 The interrupt was triggered because status bit UEBS went to ”1”

Note

To prevent the interrupt OB from being invoked twice, you must reset the relevant bit in system data 0 in the S5-150U and S5-155U (150 mode) immediately after reading the interrupt request bytes. For this the FB 42 is available to you.

Write initial count

To modify the initial count value, you must enter the new value in the transfer buffer and write job number 11_H or 21_H in the job request register.

Table 11-10. Contents of the Transfer Buffer on Writing the Initial Count, Counting Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	10^1						10^0		Initial count
1	10^3						10^2		
2	0						0		
3	0	0	0	0	0	0	0	SG	Sign of the initial count SG=1 The initial count value is negative SG=0 The initial count value is positive
4 to 14	0	. . .		0	0	. . .		0	

Write control bits

To reinitialize control bits, you must enter the new control bits in the transfer buffer and write job number $1A_H$ or $2A_H$ in the job request register.

Table 11-11. Contents of the Transfer Buffer on Writing Control Bits, Counting Mode

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	0	0	0	STRT	0	0	0	0	Control bits
1	AMSK	0	0	0	0	0	DA1F	DA1S	
2 to 14	0	. . .		0	0	. . .		0	

Description of the control bits

AMSK =1 All interrupts for the channel are masked, i.e. lost
=0 Enable interrupts

DA1F DA1S
0 0 Digital output D1 is reset
0 1 Digital output D1 is set and reset on a mode-dependent basis
1 1 Digital output D1 is set irrespective of the actual value

STRT =1 Enable counting
=0 Stop counting

11.4.3 Reading Error Messages

The IP 240 makes the error available in the transfer buffer when you transfer job number 01_H to the IP 240's job request register.

Table 11-12. Contents of the Transfer Buffer on Reading Error Messages

Offset transfer buffer	Bit 7	6	5	4	3	2	1	0	Description
0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 3
1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 3
2	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 2
3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 2
4	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Error no. 1
5	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Extension to error no. 1
6 to 14	0	. . .		0	0	. . .		0	

Error message 1 contains the most recently detected error. The error numbers are in KH format, and are reset on the IP 240 once they have been read out.

You will find a complete list of error messages in Chapter 14.

11.5 Sample Programs

The following sample programs show how to program direct data interchange with the IP 240.
Note that time monitoring of the loops for querying the IP status register has been omitted from the STEP 5 programs for the purpose of clarity and better readability. The loop counters should be set to 11 ms.

11.5.1 Reading Data from the IP 240

The module is set to start address 224 and configured for position decoding mode. You want to read the BCD-coded actual value from channel 1.

```
                  READ ACTUAL VALUE
      :
      : IA                              DISABLE INTERRUPTS
      :
      : L       KFXY                    INITIALIZE LOOP COUNTER. DEFINE XY SO THAT THE
TIME  : L       KF+1                    DELAY IN THE WAIT LOOP IS AT LEAST 200 µS.
      : -F
      : L       KF+0
      : ><F
      : TAK
      : JC      =TIME                   WAITING TIME NOT YET ELAPSED?
      :
STA1  : L       PY239                   READ STATUS REGISTER
      : T       FY239
      : A       F  239.0 -AFRT          HAS OLD JOB TERMINATED?
      : JC      =FER1
      :
      : AN      F  239.2 -DFRT          IS ″DATA READY″ BIT RESET?
      : JC      =STA1
      :
      : L       KH0040                  LOAD JOB NUMBER FOR ″RESET COMMUNICATION″
      : T       PY239                   AND TRANSFER JOB NUMBER
      :
STA2  : L       PY239                   READ STATUS REGISTER
      : T       FY239
      : AN      F  239.0 -AFRT          IS ″JOB TERMINATED″ BIT NOT YET SET?
      : JC      =STA2
      :
FER1  : A       F  239.5 -IDLE          CHANNEL 1 NOT CONFIGURED?
      : JC      =ERR1                   GENERATE ERROR MESSAGE
      :
      : A       M  239.4 -ERR           ERROR?
      : JC      =ERR3                   JUMP TO ″READ ERROR MESSAGES″
      :
      : L       KH001B                  LOAD JOB NUMBER FOR ″READ ACTUAL VAL. AND STATUS
      : T       PY239                   AREA FROM CHANNEL 1″ AND TRANSFER JOB NUMBER
      :
      :
STA3  : L       PY239                   READ STATUS REGISTER
      : T       FY239
      : AN      F  239.2 -DFRT          DATA NOT YET AVAILABLE?
      : JC      =STA3
```

```
      :  L      M  239.4 -ERR          ERROR?
      :  JC     =ERR2                  JUMP TO ”READ ERROR MESSAGES”
      :
      :  L      PY224                  TRANSFER BCD-CODED ACTUAL VALUE
      :  T      FY227
      :  L      PY225
      :  T      FY226
      :  L      PY226
      :  T      FW224                  FW224 AND FW226 CONTAIN THE ACTUAL VALUE
      :
      :  L      PY232                  TRANSFER THE SIGN OF THE ACTUAL VALUE
      :  T      FY222                  AND THE OVERRANGE STATUS BIT
      :
      :  L      KH0040                 LOAD JOB NUMBER FOR JOB TERMINATED AND
      :  T      PY239                  TRANSFER JOB NUMBER
      :
      :  RA                            ENABLE INTERRUPTS
      :
      :  BEU
      :
ERR1  :                                GENERATE AND DISPLAY ERROR MESSAGE:
      :                                CHANNEL 1 NOT CONFIGURED
      :                                E.G. ASSIGN FLAG BIT
      :
      :  RA                            ENABLE INTERRUPTS
      :
      :  BEU
      :
      :           READ ERROR BYTES
      :
ERR2  :  L      KH0040                 LOAD JOB NUMBER FOR ”RESET COMMUNICATION”
      :  T      PY239                  AND WRITE JOB NUMBER
      :
STA4  :  L      PY239                  READ STATUS REGISTER
      :  T      FY239
      :  AN     F  239.0 -AFRT         COMMUNICATION NOT YET RESET?
      :  JC     =STA4
      :
ERR3  :  L      KH0001                 LOAD JOB NUMBER FOR LOAD ERROR MESSAGES
      :  T      PY239                  AND WRITE JOB NUMBER
      :
STA5  :  L      PY239                  READ STATUS REGISTER
      :  T      FY239
      :  AN     F  239.2 -DFRT         DATA NOT YET AVAILABLE?
      :  JC     =STA5
      :
      :  L      PW224                  TRANSFER ERROR MESSAGES
      :  T      FW228                  FW228 CONTAINS ERROR MESSAGE 3
      :  L      PW226
      :  T      FW230                  FW230 CONTAINS ERROR MESSAGE 2
      :  L      PW228
      :  T      FW232                  FW232 CONTAINS ERROR MESSAGE 1
      :
      :  L      KH0040                 LOAD JOB NUMBER FOR JOB TERMINATED
      :  T      PY239                  TRANSFER JOB NUMBER
      :
      :  RA                            ENABLE INTERRUPTS
      :
      :  BE
```

11.5.2 Writing Data to the IP 240

The module is set to module address 160 and channel 2 is configured for position decoding mode. The limit values for the 3rd track were transferred to the IP 240 in the restart routine (OB20/21/22) and are to be modified in the cyclic program.
The initial track value, with sign, is in MD 140, the final track value in MD 144.

```
                  WRITE INITIAL AND FINAL TRACK VALUES
      :
      : IA                              DISABLE INTERRUPTS
      :
      : L       KFXY                    INITIALIZE LOOP COUNTER. DEFINE XY SO
TIME  : L       KF+1                    THAT THE DELAY IN THE WAIT LOOP IS AT
      : -F                              LEAST 200 µs
      : L       KF+0
      : ><F
      : TAK
      : JC      =TIME                   WAITING TIME NOT YET ELAPSED?
      :
STA1  : L       PY175                   READ STATUS REGISTER
      : T       FY239
      :
      : A       F  239.0 -AFRT          OLD JOB TERMINATED?
      : JC      =FER1
      :
      : AN      F  239.2 -DFRT          ”DATA READY” BIT RESET?
      : JC      =STA1
      :
      : L       KH0040                  LOAD JOB NUMBER FOR ”RESET COM-
      : T       PY175                   MUNICATION” AND TRANSFER JOB NO.
      :
STA2  : L       PY 175                  READ STATUS REGISTER
      : T       FY239
      :
      : AN      F  239.0 -AFRT          ”JOB TERMINATED” BIT NOT YET SET?
      : JC      =STA2
      :
FER1  : A       F  239.6 -IDLE          CHANNEL 2 NOT CONFIGURED?
      : JC      =ERR1                   GENERATE ERROR MESSAGE
      :
      : A       F  239.4 -ERR           ERROR?
      : JC      =ERR3                   JUMP TO ”READ ERROR MESSAGES”
      :
      :                                 LOAD JOB NUMBER FOR ”WRITE TRACK
TRAN  : L       KH 0023                 LIMITS FOR 3RD TRACK, CHANNEL 2”
      : L       KH 0080                 MASK FOR SETTING BIT
      : OW
      : T       PY 175                  TRANSFER ADAPTED JOB NUMBER
      :                                 TO JOB REQUEST REGISTER
      :
      : L       FY 143                  TRANSFER BCD DECADES 10^1 AND
      : T       PY 160                  10^0 OF INITIAL TRACK VALUE FOR 3RD TRACK
      :
```

```
      :  L      FY 142                TRANSFER BCD DECADES 10^3 AND 10^2
      :  T      PY 161                OF THE INITIAL VAL. FOR THE 3RD TRACK
      :
      :  L      FY 141                TRANSFER BCD DECADE 10^4 OF THE
      :  T      PY 162                INITIAL VAL. FOR THE 3RD TRACK
      :
      :  L      FY 140                TRANSFER SIGN OF INITIAL VALUE
      :  T      PY 163                FOR THE 3RD TRACK
      :
      :  L      FY 147                TRANSFER BCD DECADES 10^1 AND 10^0
      :  T      PY 164                OF THE FINAL VAL. FOR THE 3RD TRACK
      :
      :  L      FY 146                TRANSFER BCD DECADES 10^3 AND 10^2
      :  T      PY 165                OF THE FINAL VAL. FOR THE 3RD TRACK
      :
      :  L      FY 145                TRANSFER BCD DECADE 10^4 OF THE
      :  T      PY 166                FINAL VAL. FOR THE 3RD TRACK
      :
      :  L      FY 144                TRANSFER SIGN OF THE FINAL
      :  T      PY 167                VAL. FOR THE 3RD TRACK
      :
      :  L      KH 0023               LOAD JOB NO.FOR "WRITE TRACK
      :  T      PY 175                LIMITS FOR 3RD TRACK, CHANNEL 2"
      :                               AND TRANSFER THE JOB NUMBER
      :
STA3  :  L      PY 175                READ STATUS REGISTER
      :  T      FY 239
      :
      :  AN     F 239.2 -DFRT         DATA NOT YET FETCHED?
      :  JC     =STA3
      :
      :  A      M 239.4 -ERR          ERROR?
      :  JC     =ERR2                 JUMP TO "READ ERROR MESSAGES"
      :
      :  L      KH 002D               LOAD JOB NUMBER FOR "TERMINATE DATA
      :  T      PY 175                INTERCHANGE WITH CHANNEL 2" AND
      :                               TRANSFER JOB NUMBER
      :  RA                           ENABLE INTERRUPTS
      :
      :  BEU

ERR1  :                               GENERATE AND DISPLAY ERROR MESSAGE:
      :                               CHANNEL 2 NOT CONFIGURED
      :                               E.G. ASSIGN FLAG BIT
      :
      :  RA                           ENABLE INTERRUPTS
      :
      :  BEU
      :
      :           READ ERROR MESSAGES
      :
ERR2  :  L      KH0040                LOAD JOB NUMBER FOR "RESET COM-
      :  T      PY175                 MUNICATION" AND TRANSFER JOB NUMBER
      :
STA4  :  L      PY175                 READ STATUS REGISTER
      :  T      FY239
      :
      :  AN     F  239.0 -AFRT        COMMUNICATION NOT YET RESET?
      :  JC     =STA4
```

```
ERR3  : L     KH0001               LOAD JOB NUMBER FOR ”LOAD ERROR
      : T     PY175                MESSAGES” AND TRANSFER JOB NO.
      :
STA5  : L     PY175                READ STATUS REGISTER
      : T     FY239
      :
      : AN    F  239.2 -DFRT       DATA NOT YET AVAILABLE?
      : JC    =STA5
      :
      : L     PW160                TRANSFER ERROR MESSAGES
      : T     FW228                FW228 CONTAINS ERROR MESSAGE 3
      : L     PW162
      : T     FW230                FW230 CONTAINS ERROR MESSAGE 2
      : L     PW164
      : T     FW232                FW232 CONTAINS ERROR MESSAGE 1
      :
      : L     KH0040               LOAD JOB NUMBER FOR ”JOB
      : T     PY175                TERMINATED” AND TRANSFER JOB NO.
      :
      : RA                         ENABLE INTERRUPTS
      :
      : BE
```

Figures

Tables

12 Response Times

The response time is the time between reaching of a setpoint and the IP 240's reaction.

The signals from the incremental encoders or pulse encoders are acquired by counter chips. These counter chips make an internal count available which is read and evaluated in each module firmware (FW) cycle. IP inputs IN and GT are also sensed at the hardware level and postprocessed by the firmware.

All evaluations in which the IP 240 firmware is involved are, as regards their response time, determined by the cycle time of the module firmware. The cycle time itself depends on:
- the modes in which the channels are operated,
- the configuring data,
- the current actual value and
- the requests for data interchange with the S5 CPU.

12.1 Structure of a Firmware Cycle

A firmware cycle is subdivided into slices for
- processing of channel 1
- processing of channel 2
- data interchange

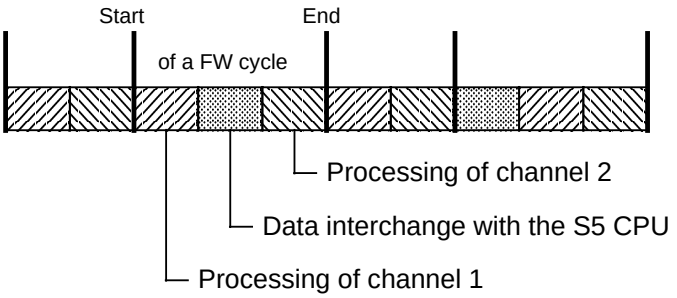


Figure 12-1. Structure of a Firmware Cycle (Example)

When processing of a channel begins, the data acquired at the hardware level is read in by the firmware. Because the IP 240 firmware has a free-wheeling cycle, this is not done in a fixed time-slot pattern, but rather is dependent on the processing times of the slices for ”Processing of channel 1”, ”Processing of channel 2” and ”Data interchange with the S5 CPU”.

No more than one data interchange with the S5 CPU may take place in a firmware cycle. Once new data have been transferred to the IP 240, the next FW cycle is closed to data interchange.
A pending request is processed as soon as possible. The data interchange can thus be carried out at different points within the firmware cycle.

The data made available by the IP 240 is always based on the last count read, and is **not** updated again when a data interchange takes place.

12.2 Computing the Response Time

Using channel 1 as example, Figure 12-2 shows which FW slices must be taken into account when computing the response time.

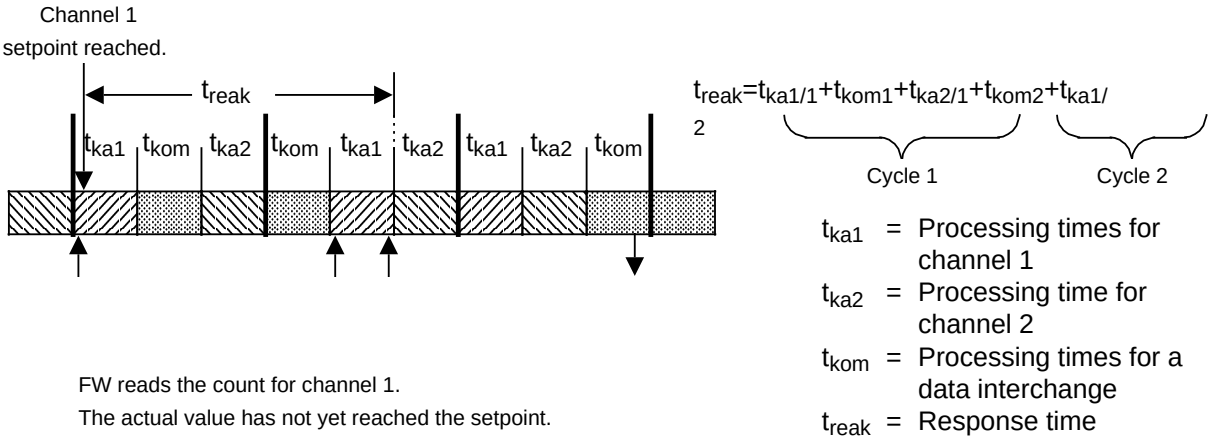


Figure 12-2. Computing the Response Time

The maximum response times are thus as follows:

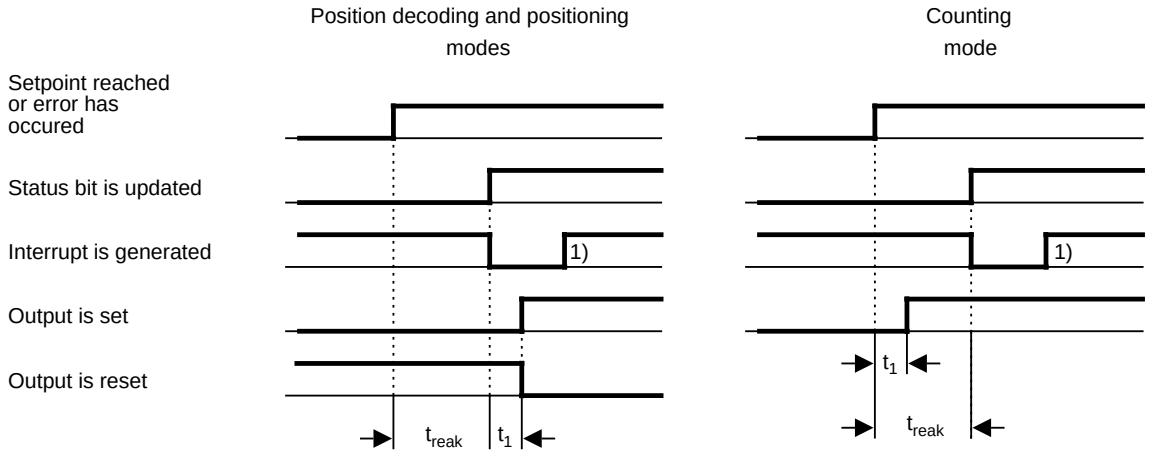
for channel 1 $t_{reak.\text{-}ka1\ max.} = t_{ka1/1\ max.} + t_{ka2/1\ max.} + t_{kom1\ max.} + t_{kom2\ max.} + t_{ka1/2\ max.}$

for channel 2 $t_{reak.\text{-}ka2\ max.} = t_{ka2/1\ max.} + t_{kom1\ max.} + t_{ka1/2\ max.} + t_{kom2\ max.} + t_{ka2/2\ max.}$

Substitute the maximum value for a data Read for $t_{kom1\ max.}$ and the maximum value for a data Write for channel 1 or channel 2 for $t_{kom2\ max.}$ If the IP 240 is not accessed during positioning or during a counting cycle, assume $t_{kom}=0$.

The new data are available on the IP 240 when the response time has elapsed, and can be read out with the next data interchange.

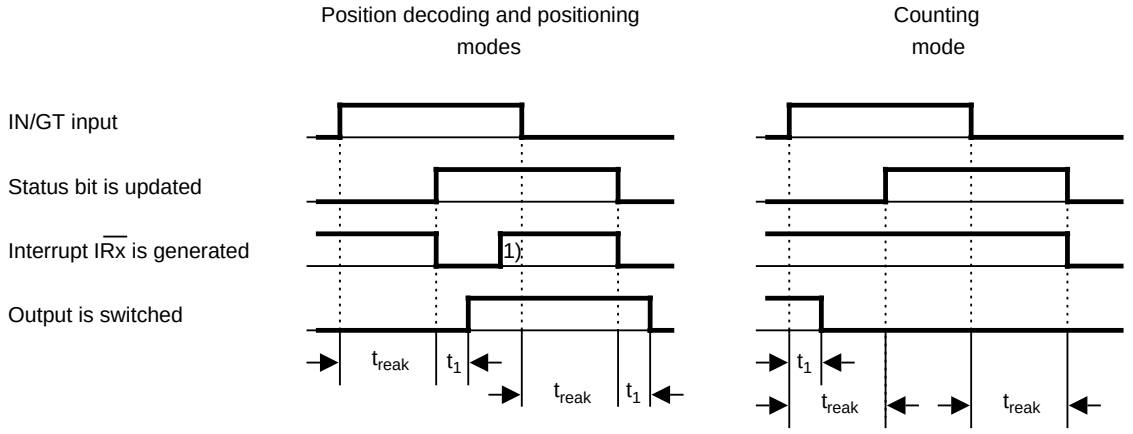
The execution times of the individual slices are discussed in detail in Section 12.3.



t_1=max. 50 µs (when ohmic load and I_{output}=50 mA)

1) Is reset following reading of the interrupt request bytes

Fig. 12-3. Response Time for Evaluation of the Actual Value and of Wirebreak and Zero Mark Errors



t_1=max. 50 µs (when ohmic load and I_{output}=50 mA)

1) Is reset following reading of the interrupt request bytes

Fig. 12-4. Response Time for Evaluation of Inputs IN and GT

Note

Switching of the IP outputs is

- firmware-controlled in position decoding and positioning mode.
- counter chip controlled in counting mode and thus independent of the module firmware's response time.

12.3 Firmware Execution Times

The execution time of the individual firmware slices depends on
- the modes in which the channels are operated,
- the configuring data and
- the current actual value.

The table below shows the
- base times which the firmware needs in each cycle to process channel 1 and channel 2.
- the additional times needed only in the firmware cycle in which the setpoint is reached or in which an error occurs.
- the execution time for a data interchange in the relevant mode.

When computing the response time, you must always assume the maximum value for a data interchange.

Position decoding mode

Table 12-1. Firmware Execution Times, Position Decoding Mode

Description	Abbrev.	Max. execution time
Base time without configuring	t_A	45 µs
Base time for position decoding without track comparison	t_W	520 µs
Base time per track comparison without hysteresis Base time per track comparison with hysteresis	t_{WS1} t_{WS2}	160 µs 230 µs
Additional time for entering and exiting a track	t_{WZ1}	30 µs
Additional time for IP 240 to set or reset an output (per DQ)	t_{WZ2}	45 µs
Additional time for IP 240 to generate an interrupt (for each interrupt bit set)	t_{WZ3}	30 µs
Time for a data exchange Data Read Data Write	 t_{kom} t_{kom}	 430 µs 740 µs

Example:

Channel 1:
- Base time without configuring — t_A = 45 µs
- Position decoding modes — t_W = 520 µs
- 6 tracks used, without hysteresis — 6 x t_{WS1} = 960 µs

In one FW cycle,
- a track can be entered, — t_{WZ1} = 30 µs
- an output set and the other output reset and — 2 x t_{WZ2} = 90 µs
- an actual value-dependent interrupt generated. — t_{WZ3} = 30 µs

t_{ka1} = 1675 µs

Channel 2:	• Base time without configuring		t_A	=	45	µs
	• Position decoding mode		t_{WW}	=	520	µs
	• 8 tracks used, without hysteresis	8 x	t_{WS2}	=	1840	µs
	In one FW cycle,					
	• two tracks can be entered,	2 x	t_{WZ1}	=	60	µs
	• both outputs can be switched,	2 x	t_{WZ2}	=	90	µs
	• two actual value-dependent interrupts can be generated,	2 x	t_{WZ3}	=	60	µs
	• and the DRBR signal can trigger an interrupt.		t_{WZ3}	=	30	µs
					---	
			t_{ka2}	=	2645	µs

Counting mode

Table 12-2. Firmware Execution Times, Counting Mode

Description	Abbrev.	Max. execution time
Base time without configuring	t_A	45 µs
Base time for counting	t_Z	470 µs
Additional time for IP 240 to generate an interrupt (for each interrupt bit set)	t_{ZZ1}	30 µs
Time for a data exchange Data Read Data Write	 t_{kom} t_{kom}	 440 µs 560 µs

Example:

Channel 1:	• Base time without configuring		t_A	=	45	µs
	• Counting mode		t_Z	=	470	µs
	• Two interrupts can generated in each FW cycle.	2 x	t_{ZZ1}	=	60	µs
					---	
			t_{ka1}	=	575	µs

Channel 2:	• Base time without configuring (channel not used)		t_A	=	45	µs
					---	
			t_{ka2}	=	45	µs

Positioning mode

Table 12-3. Firmware Execution Times, Positioning Mode

Description		Abbrev.	Max. execution time
Base time without configuring		t_A	45 µs
Base time for positioning with linear axis and ZYSY=0 Base time for positioning with rotary axis and ZYSY=0		t_{PL1} t_{PR1}	1050 µs 1100 µs
Base time for positioning with linear axis and ZYSY=1 Base time for positioning with rotary axis and ZYSY=1		t_{PL2} t_{PR2}	1250 µs 1550 µs
Additional time for entering and exiting a range		t_{PZ1}	80 µs
Additional time for IP 240 to set or reset an output (per DQ)		t_{PZ2}	25 µs
Additional time for IP 240 to generate an interrupt (for each interrupt bit set)		t_{PZ3}	30 µs
Time for			
reading binary data	(BCD/y=0)	t_{kom}	240 µs
reading BCD data	(BCD/y=1)	t_{kom}	520 µs
writing binary data	(BCD/y=0 and BCD/x=0)	t_{kom}	960 µs
writing BCD data	(BCD/y=1 or BCD/x=1)	t_{kom}	1650 µs

Example:

Channel 1:
- Base time without configuring — t_A = 45 µs
- Positioning mode, linear axis with ZYSY=0 — t_{PL1} = 1050 µs

In one FW cycle,
- two ranges can be entered, — 2 x t_{PZ1} = 160 µs
- both outputs can be switched, — 2 x t_{PZ2} = 50 µs
- two actual value-dependent interrupts can be generated — 2 x t_{PZ3} = 60 µs
- and the DRBR signal can trigger an interrupt. — t_{PZ3} = 30 µs

t_{ka1} = 1395 µs

Channel 2:
- Base time without configuring — t_A = 45 µs
- Positioning mode, linear axis with ZYSY=1 — t_{PL2} = 1250 µs

In one FW cycle,
- one range can be entered, — t_{PZ1} = 80 µs
- both outputs can be switched, — 2 x t_{PZ2} = 50 µs
- one actual value-dependent interrupt can be generated — t_{PZ3} = 30 µs
- and storing of the final value can trigger an interrupt. — t_{PZ3} = 30 µs

t_{ka2} = 1485 µs

Figures

13 Encoder Signals

This section discusses the requirements for the forms and timing of the signals for the IP 240. The following encoder signals are discussed in this section:

- Incremental encoder signals for position decoding, IP 252 expansion and positioning mode (Section 13.1).
- The signal at binary input IN for reference point approach and for synchronization with an external control signal for position decoding and positioning mode (Section 13.2).
- The signals at counting input CLK and at binary input GT for counting mode (Section 13.3).

13.1 Signal Forms and Timing Requirements for Incremental Encoders

13.1.1 Signal Forms

In position decoding, IP 252 expansion and positioning mode, the incremental encoders used for producing position-dependent signals must generate two square-wave pulse trains in quadrature. If you want to execute a reference point approach in position decoding and positioning mode, at least one high-active zero mark signal (reference signal) per encoder revolution is also required.

You can connect incremental encoders to the IP 240 which generate

- symmetrical signals A/$\overline{A}$, B/$\overline{B}$ and Z/$\overline{Z}$; the IP interface for these encoders conforms as regards the level to the RS 422A standard.
- asymmetrical signals A*, B* and Z* with a rated encoder voltage of 5 V or 24 V.

To match the IP 240 to the type of encoder and the signal level, you must set coding switches S4, S5 and S6 (Section 5.3).

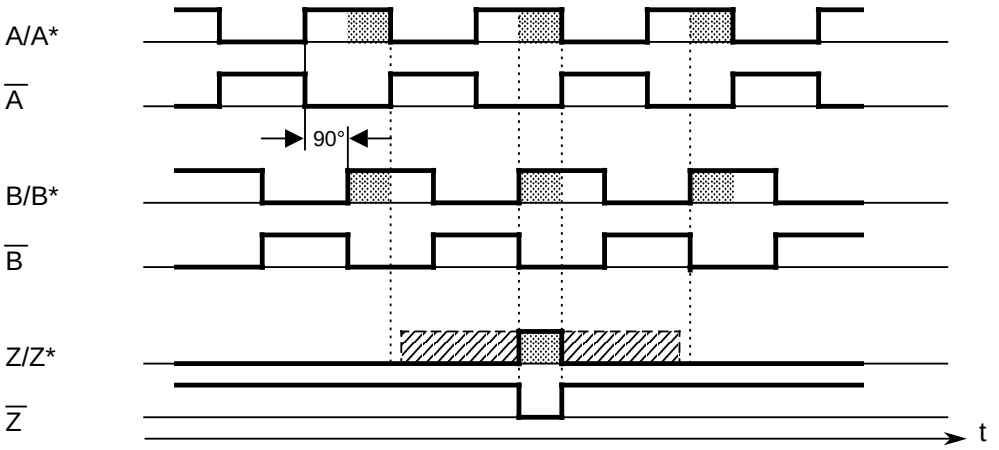


Fig. 13-1. Signal Forms: Symmetrical Encoder Signals $\overline{A}$/A, $\overline{B}$/B, $\overline{Z}$/Z Asymmetrical Encoder Signals A*, B*, Z*

Note

To change the counting direction, you must interchange the connections as follows:

- for symmetrical encoders, interchange A/A $\overline{}$ with B/B $\overline{}$
- for asymmetrical encoders, interchange A* with B*

13.1.2 Timing Requirements

The following diagrams show the timing requirements for signals A, B and Z at the IP 240's inputs. These requirements must be observed in order to enable proper evaluation of the signals.

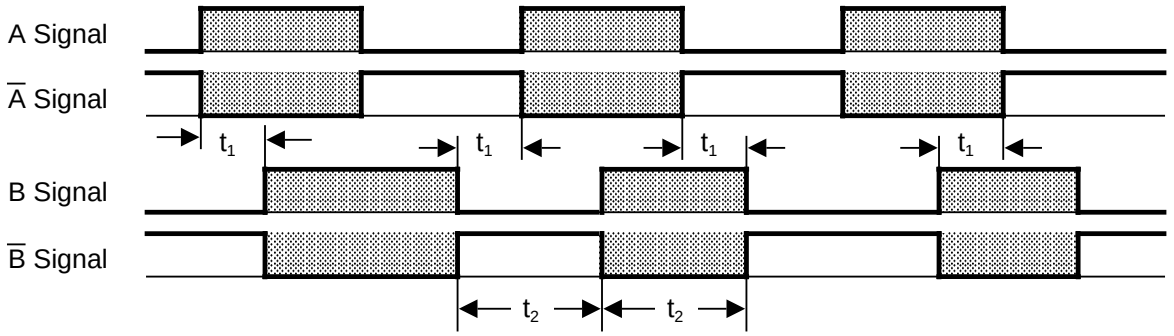
Z signal
During reference point approach and zero mark monitoring, the Z signal is evaluated while A=1 and B=1. The state A=1 and B=1 may occur only once for the duration of the Z signal (Z=1). In addition, one of the following conditions must be satisfied to ensure that the correct edge of the Z signal is used in every instance:

- When using a symmetrical encoder, the Z signal must go to ”1” no more than 250 ns (t_5) after the last positive signal edge of pulse train A or B (Fig. 13-2c).
- When using an asymmetrical encoder, the Z signal must go to ”1” at least 2.5 µs (t_5) before the pending positive signal edge of pulse train A* or B* (Fig. 13-3b).

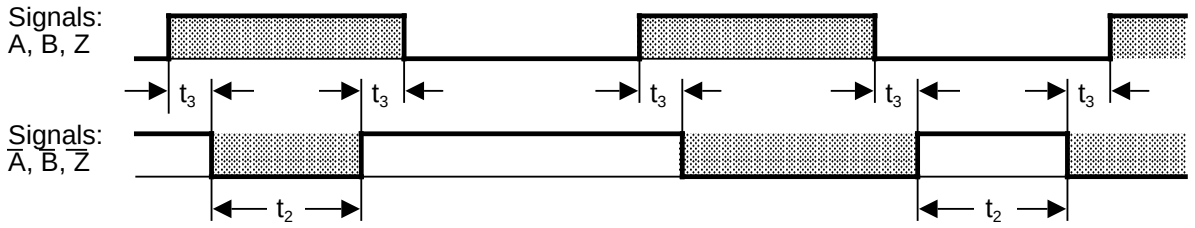
When your encoder can maintain this timing only in one direction of rotation, the reference point must be approached with this direction of rotation. Zero mark monitoring is then carried out in this direction only.
When the encoder cannot maintain this timing, you must disable zero mark monitoring during configuring (configuring parameter IMP=0).

Timing requirements for encoders with symmetrical signals

a) Skew between tracks A and B (minimum edge spacing):



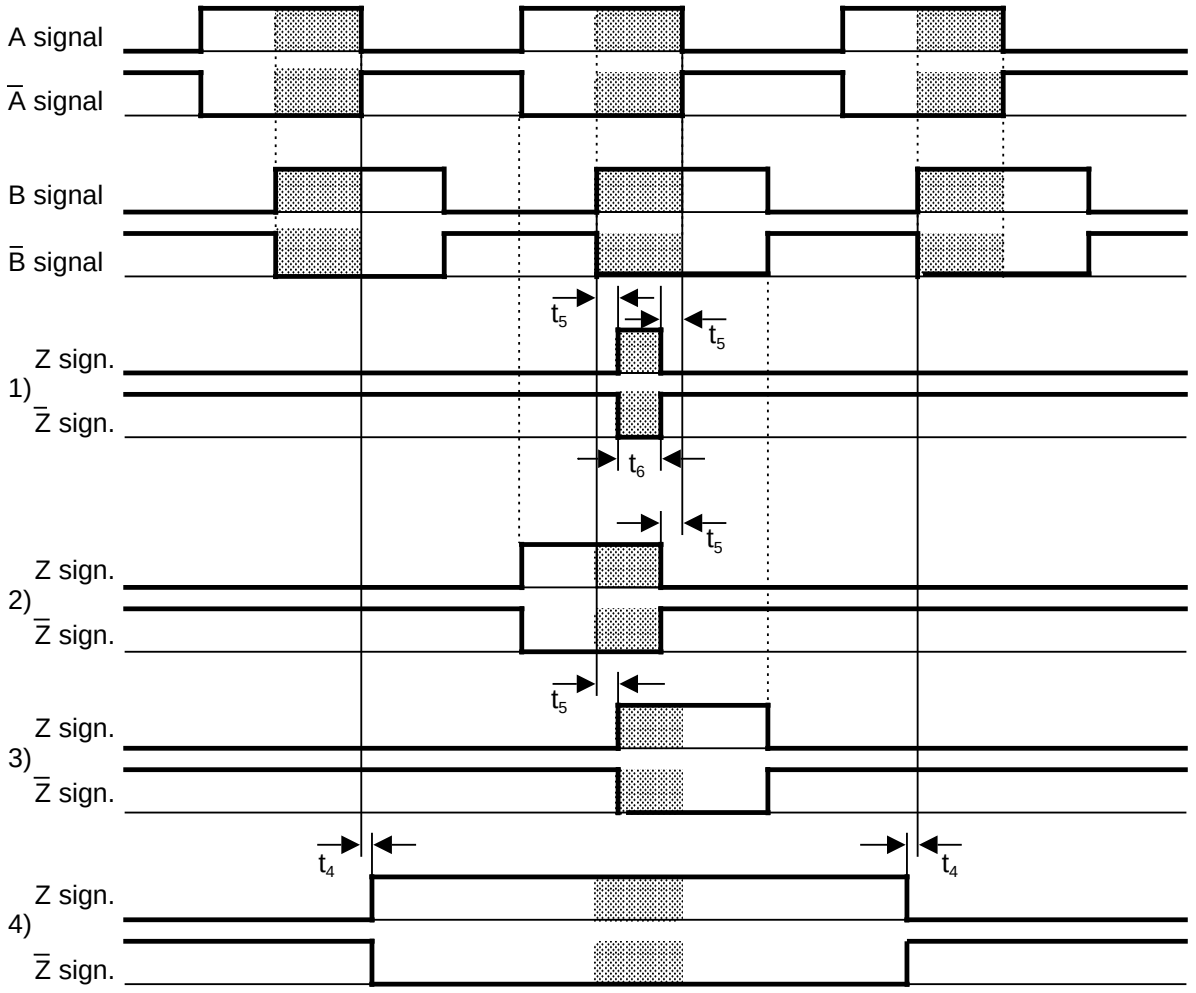
b) Skew between the signals of a track:



t_1: min. 500 ns t_2: min. 1 µs t_3: max. 20 ns

Fig. 13-2. Timing Diagrams for Symmetrical Incremental Encoders

c) Position and timing of the Z signal:



t_4: min. 50 ns t_5: max. 250 ns t_6: min. 500 ns

1) Position of the Z signal at minimal signal length
2) Position of the Z signal when the Z signal corresponds to the A signal
3) Position of the Z signal when the Z signal corresponds to the B signal
4) Position of the Z signal at maximum signal length

An edge steepness of at least 5 V/µs is required for all signals.

Fig. 13-2. Timing Diagram for Symmetrical Incremental Encoders (Continued)

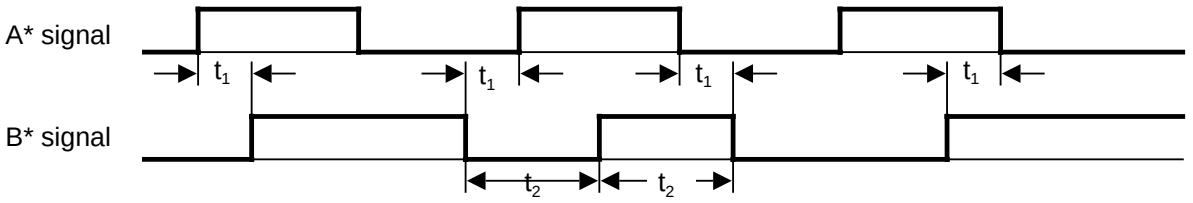
If the encoder has no $\overline{Z}$ signal, the $\overline{Z}$ input of a symmetrical encoder must be applied to a 1 signal and the Z input to a 0 signal.

Note

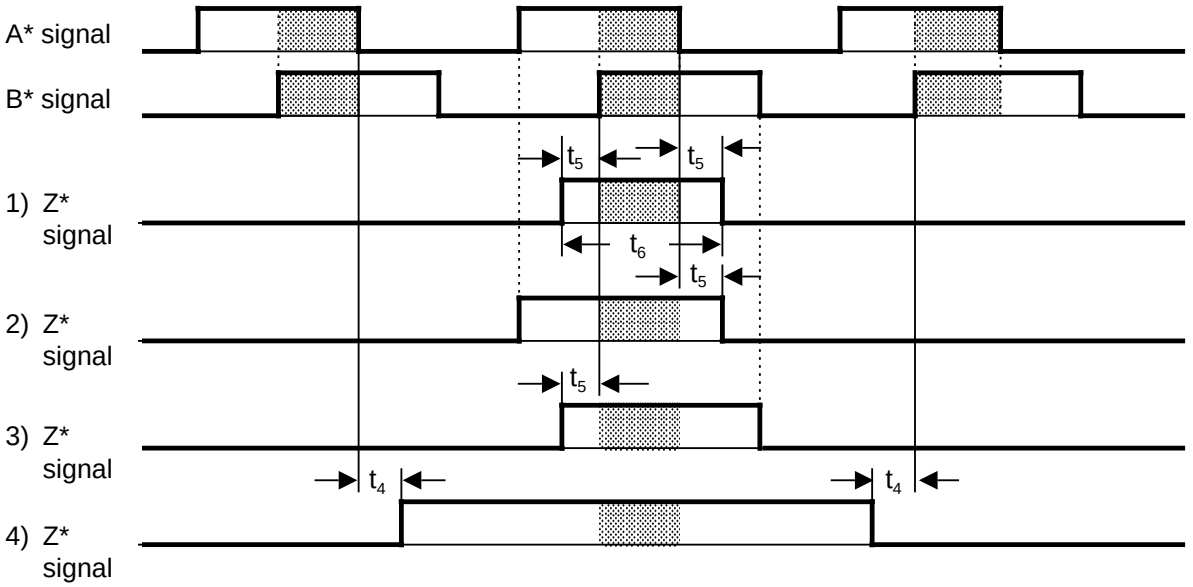
The requirements regarding the position of the Z signal do not apply to IP 252 expansion mode, as neither reference point approach nor zero mark monitoring is possible in this mode.

Timing requirements for encoders with asymmetrical signals

a) Skew between tracks A and B (minimum edge spacing):



b) Position and timing of the Z signal:



t_1: min. 2.5 µs t_2: min. 5.0 µs t_4: min. 2.5 µs t_5: min. 2.5 µs t_6: min. 7.5 µs

1) Position of the Z signal at minimal signal length
2) Position of the Z signal when the Z signal corresponds to the A signal
3) Position of the Z signal when the Z signal corresponds to the B signal
4) Position of the Z signal at maximum signal length

Fig. 13-3. Timing Diagram for Asymmetrical Encoders

13.2 Timing at Binary Input IN

Binary input IN is used as preliminary contact signal during reference point approach in position decoding and positioning mode. For positioning with external synchronization, this input is also used for connecting the synchronization signal.
Only bounce-free 5 V or 24 V encoders are permissible.

The IN signal is evaluated by the IP 240 module firmware. For this reason, acquisition of the signal edges may sometimes be deferred by one firmware cycle.

The times and edge steepness given below refer to the signals present on the module.

Connection of the preliminary contact signal to the IN input

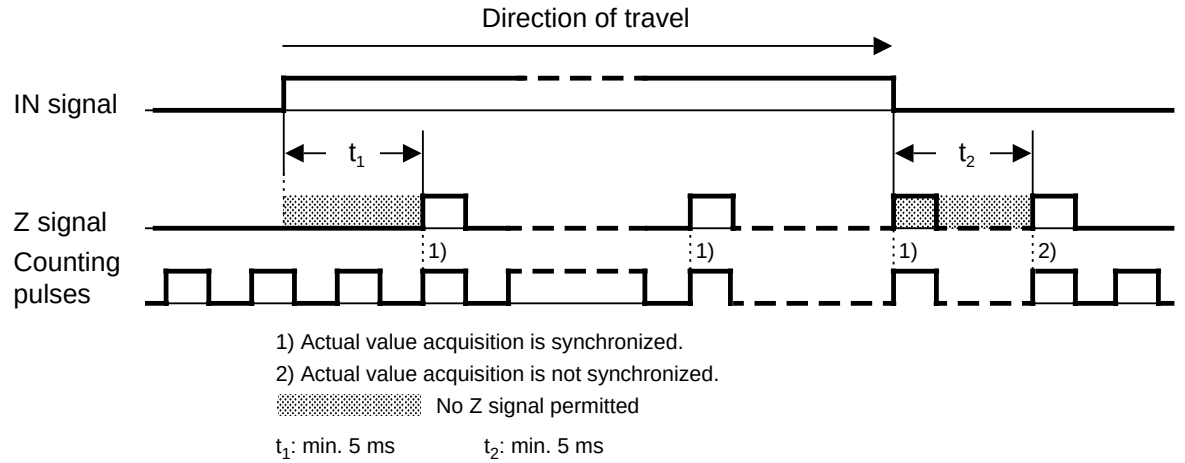


Fig. 13-4. Timing Diagram for Reference Point Approach, Position Decoding Mode

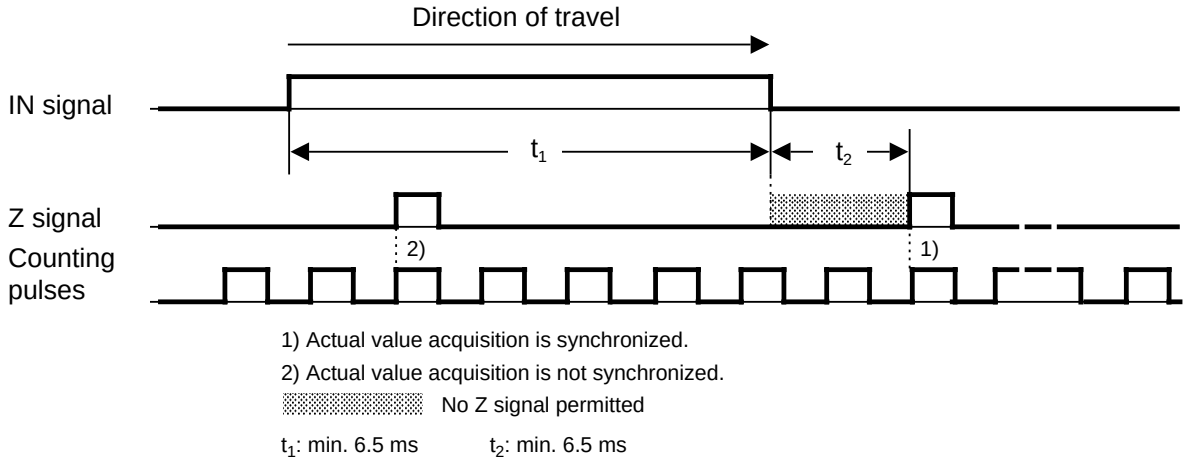
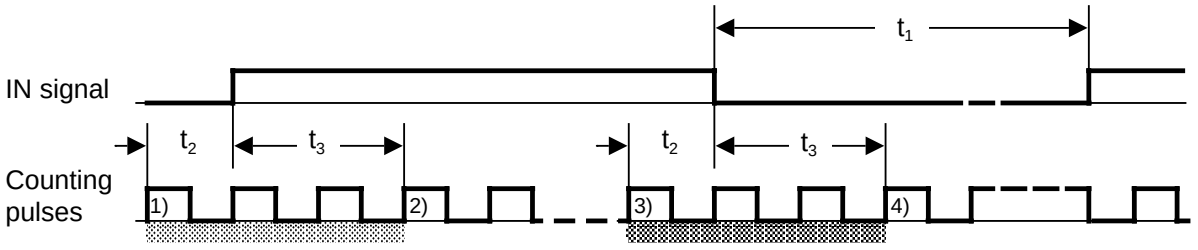


Fig. 13-5. Timing Diagram for Reference Point Approach, Positioning Mode

Note

It must be ensured that synchronization always takes place at the same zero mark position by selecting the traversing speed during reference point approach and aligning the preliminary contact signal edges between the zero marks.

Connecting the synchronization signal to the IN input



1) Pulse is not taken into account for new counting cycle.
2) Pulse is counted in next counting cycle.
3) Pulse is taken into account in stored final value.
4) Pulse is not taken into account in stored final value

These pulses can be counted for the actual value before or after the positive IN edge.

These pulses can be counted for the actual value before or after the negative IN edge.

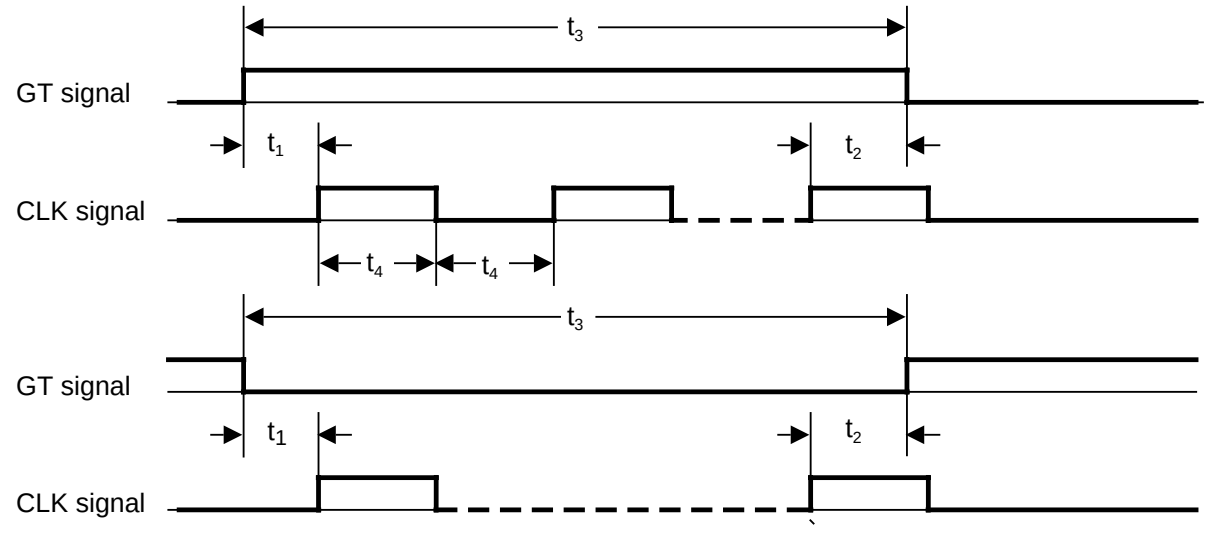
t_1 : min. 7.5 ms t_2 : min. 500 µs t_3 : min. 7.0 ms

Fig. 13-6. Timing Diagram for the Synchronization Signal, Positioning Mode

13.3 Timing at Counting Input CLK and at Binary Input GT

Signal inputs CLK (clock) and GT (gate) are used in counting mode.
Only bounce-free 24 V encoders may be used. Coding switches S5 and S6 must be set to 24 V. It is also possible to connect 3-wire and 4-wire BERO proximity switches.
Because the GT signal is also evaluated by the IP 240 module firmware, care must be taken that the signal be present for at least 5 ms as active signal and 5 ms as inactive signal. The maximum frequency is 100 Hz.
To enable defined counter operation, times t_1 and t_2 must be carefully observed for the first CLK signal while GT=1 or GT=0.

The times and edge steepness given below refer to the signals present on the module.



t_1: min. 2,5 µs t_2: min 2.5 µs t_3: min. 5 ms t_4: min. 5 µs

Fig. 13-7. Timing Diagram for the CLK and GT Signals, Counting Mode

Tables

14 Error Messages

If you use standard FBs 167 to 173 for data interchange between S5 CPU and IP 240, you can ascertain whether an error or fault occurred and obtain information on where you can find a more detailed error description by evaluating the PAFE byte. PAFE should be evaluated following every FB call.

Table 14-1. Errors Flagged in the PAFE Byte

Bit number in PAFE byte	HEX	Type of error	Detailed description in DB
0	01_H	Hardware, communications and data errors	DW 8 to10
1	02_H	Parameter and data errors	DW 13
2	04_H	Illegal data block no., no such data block, or data block too short, CPU not permissible	-
3	08_H	Start or continuation of data interchange with the IP 240 not possible. Waiting time for communication with IP 240 exceeded.	-
7	80_H	Function block prematurely aborted	-

If you program data interchange between S5 CPU and IP 240 yourself, you must scan the ERR bit after reading the IP 240's status register and read out the error messages from the IP 240 if this bit is ”1” (Chapter 11, ”Direct Data Interchange”).

> **Note**
>
> All error messages are in KH format.

14.1 Hardware Faults

Some hardware components are checked via a test routine following power-up. If a fault is detected, the IP 240 sets the red MF LED. You can read out the error message from the IP 240 by invoking a configuring FB. The FB enters the error codes in DW 8 to 10 of the specified data block.

Table 14-2. Hardware Faults

Error code (DW 8 to 10)	Description
1001	Watchdog error
1002	Error in checksum test (EPROM)
1003	Error in counter test (82C54)
101n	Error detected in RAM test no. n (n=1 to 8)
102n	Error detected in transfer buffer test no. n (n=1 to 8)

14.2 Error Messages in Position Decoding and Counting Mode

14.2.1 Parameter and Data Errors

In position decoding and counting mode, the FB parameter and the DB data are checked by the standard function blocks. If an error is detected, the error code is entered in DW 13 of the specified data block.

Table 14-3. Parameter and Data Errors in Position Decoding and Counting Mode

Error code (DW 13)	Description
0001	Illegal module address
0002	Illegal channel number
0003	Error in configuring parameter
0004	FB incompatible with IP firmware
0101	Invalid initial value for track 1
0102	Invalid initial value for track 2
0103	Invalid initial value for track 3
0104	Invalid initial value for track 4
0105	Invalid initial value for track 5
0106	Invalid initial value for track 6
0107	Invalid initial value for track 7
0108	Invalid initial value for track 8
0111	Invalid final value for track 1
0112	Invalid final value for track 2
0113	Invalid final value for track 3
0114	Invalid final value for track 4
0115	Invalid final value for track 5
0116	Invalid final value for track 6
0117	Invalid final value for track 7
0118	Invalid final value for track 8
0120	Invalid zero offset
0121	Invalid hysteresis
0122	Invalid initial count
0201	Limit values for track 1 cannot be transferred *
0202	Limit values for track 2 cannot be transferred *
0203	Limit values for track 3 cannot be transferred *
0204	Limit values for track 4 cannot be transferred *
0205	Limit values for track 5 cannot be transferred *
0206	Limit values for track 6 cannot be transferred *
0207	Limit values for track 7 cannot be transferred *
0208	Limit values for track 8 cannot be transferred * * Limit values cannot be transferred because track not configured
0210	Channel not configured
0211	Control FB illegal for configured mode or data block
0212	Illegal function number (FKT)
0213	Illegal control bit combination

14.2.2 Communications Errors

Communications errors can occur when you interchange data directly with the IP 240 without using control function blocks. You must read these errors out from the IP 240's transfer buffer (Chapter 11, ”Direct Data Interchange”).

Table 14-4. Communications Errors in Position Decoding and Counting Mode

Error code (transfer buffer)	Description
4000	Protocol error
41nn	Illegal job number, nn=old job number
420n	Error during transfer of track limits, n=number of the track

14.3 Error Messages in IP 252 Expansion Mode

Parameter errors
FB 173 checks the configuring parameters and enters errors, if any, in DW 13.

Table 14-5. Parameter Errors in IP 252 Expansion Mode

Error code (DW13)	Description
0001	Illegal module address
0003	Error in configuring parameter
0004	FB not compatible with IP firmware

14.4 Error Messages in Positioning Mode

14.4.1 Parameter Errors

In positioning mode, the initialized parameters are checked by the configuring FB and the control FB; during configuring, the value in DW 58 is also checked. When an error is detected, the error code is entered in DW 13.

Table 14-6. Parameter Errors in Positioning Mode

Error code (DW13)	Description
0001	Illegal module address
0002	Illegal channel number
0003	Error in configuring parameter
0004	FB not compatible with IP firmware
0123	Number of positions in DW 58 exceeds 254
0210	Channel not configured
0211	Control FB illegal for configured mode or for data block
0212	Illegal function number (FKT)

14.4.2 Data Errors

The specified data is checked by the module firmware. If standard function blocks are used for data interchange, the FB reads the error messages out from the IP 240 and enters the codes in data words 8 to 10.
If you program direct data interchange yourself, you must read out the error messages from the transfer buffer. The layout of the error codes and extensions is shown in Chapter 11, ”Direct Data Interchange”.

Table 14-7. Data Errors in Positioning Mode

Error code for		Extension	Description
Chan. 1	Chan. 2		
50	80	nn	Specified position number not defined when channel was configured.
		nn	=specified position number
51	81	00	Attempt made to store position 0 on the IP 240 or to call position 0 via the position number. Position number 0 can be specified via the position value only.
52	82	nn	Negative position value specified for a rotary axis or position value exceeds permissible maximum value (=final value - 1). Change the position value
		nn	=associated position number
53	83	nn	Position number and control bit HASY specified.
		nn	=specified position number
54	84	nn	Position number assigned more than once Use different position number
		nn	=specified position number
55	85	nn	Position value for linear axis out of range
		nn	=position number
58	88	nn	Synchronization mode selected although status bit DRBR (wirebreak) still set Rectify error and read status area from IP 240
		nn	=00 HASY selected =01 ZYSY selected =02 SOSY selected
59	89	nn	Position specified although actual value acquisition not yet synchronized.
		nn	=specified position number

Table 14-7. Data Errors in Positioning Mode (Continued)

Error code for Chan. 1	Error code for Chan. 2	Extension	Description
60	90	nn	Position number specified together with control bit HAND
		nn	=specified position number
61	91	nn	Invalid combination of control bits FREI, HAND, DA1S and DA2S.
		nn	=00 Control bits DA1S and DA2S in conjunction with HAND=1 illegal for configuring parameter DAV =02 HAND=1 and FREI=1 transferred for reference point approach or direction of travel not correctly specified via DA1S or DA2S and DAV=2
62	92	nn	Contents of data block or transfer buffer invalid Check contents and enter "0" in all unused positions
		nn	=00 Error while transferring zero offset =01 Error while transferring control bits =02 Error while transferring position values =03 Error while transferring distance values =04 Error while transferring position 0
63	93	nn	Illegal value specified as BCD number.
		nn	=01 Error in position value transferred =02 Error in distance value transferred =03 Error in zero offset transferred =04 Error in final value for rotary axis
64	94	nn	Certain control bits and data can be specified only when IP outputs are reset. Check the states of the IP outputs
		nn	=00 Error when selecting a position from 1 to 254 =01 Error on transferring zero offset =02 Error on selecting HASY =04 Error on selecting HAND =05 Error on transferring position values =06 Error on transferring distance values

Table 14-7. Data Errors in Positioning Mode (Continued)

Error code for		Extension	Description
Chan. 1	Chan. 2		
65	95	nn	More than one synchronization mode selected.
		nn	= 00 HASY set = 01 ZYSY set = 02 SOSY set
69	99	nn	Illegal data
		nn	= 00 Zero offset out of range = 01 Zero offset exceeds final value of rotary axis = 02 Illegal final value for rotary axis = 03 BEE1 illegal = 04 BEE2 illegal = 05 BEE3 illegal = 06 BEE1 illegal for position 0 = 07 BEE2 illegal for position 0 = 08 BEE3 illegal for position 0

14.4.3 Communications Errors

Communications errors can occur on direct data interchange with the IP 240. You must read out the error code and extension from the IP 240's transfer buffer (Chapter 11, ”Direct Data Interchange”).

Table 14-8. Communications Errors in Positioning mode

Error Code (transfer buffer)	Description
4000	Protocol error
41nn	Illegal job number, nn=old job number

Adapter Casing (S5 Adapter)

A

In this Chapter

In this chapter, you will learn

- how to install modules in the adapter casing, and
- what you must observe when using the various S5 modules.

A.1 Prerequisites

General

The following prerequisites must be observed as regards the use of S5 modules in the S7-400:

- Check with your local Siemens office that the modules you want to use have been approved for implementation.
- Programmable S5 modules can be linked into a STEP 7 user program only with special standard function blocks. Should you have only standard S5 function blocks for your S5 modules which are not expressly authorized for STEP 7 implementation in the associated documentation (Manual or Product Information), you must order new standard function blocks for those modules.
- SIMATIC S5 and SIMATIC S7 differ from one another in their general technical specifications, most particularly those relating to ambient conditions. When installing an S5 module in an S7-400, the most stringent ambient conditions for either the S5 and S7 apply for the system as a whole.

Permissible Racks

The adapter casing may be installed only in the S7-400 central rack.

Note

Before installing an S5 module which has been used in an S5 configuration in an S7 system, always call your local Siemens office for particulars. The information provided in this chapter relates exclusively to the current versions and revision level of the S5 modules covered.

A.2 Installing an Adapter Casing in the S7-400

Introductory Remarks

To install an S5 module in an S7-400, you must first install the adapter casing in the S7 rack, then set the address on the S5 module, and, finally, insert the module in the adapter casing.

Installing the Adapter Casing in a Rack

Proceed as follows to install an adapter casing in a rack:

1. Check to make sure that the jumpers on the back of the adapter casing are closed (factory setting). These jumpers are for testing purposes only, and must always remain closed.
   Figure A-1 shows the location of the jumpers.

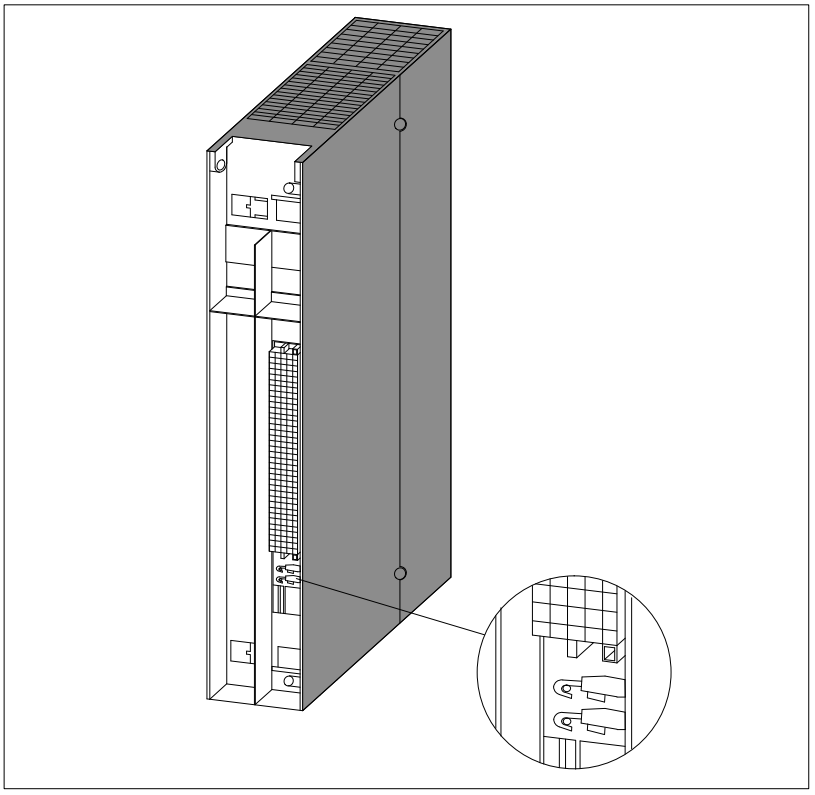


Bild A-1 Location of the Jumpers on the Adapter Casing

2. Set the CPU mode switch to the STOP position.
3. Set the standby switch on the power supply module to the ⏻ position (0 V output voltages).
4. Follow the directions in the “S7-400 and M7-400 Installation and Hardware” Manual for inserting modules in a rack.

Setting the Address

Set the address on the S5 module.

A.3 Inserting S5 Modules in the Adapter Casing

Procedure

Proceed as follows to insert an S5 module in the adapter casing:

1. Set an interrupt circuit on the module, which sets the destination CPU for interrupts (in the case of interrupt-generating modules only).

Interrupt Circuit...	... Corresponds to Destination CPU
/INT A	CPU 1
/INT B	CPU 2
/INT C	CPU 3
/INT D	CPU 4

2. Unscrew and remove the interlocking plate on the adapter casing.
3. Insert the module in the adapter casing's guide tracks and push.
   The rear plug connectors snap into the adapter casing's socket connectors.
4. Screw the interlocking plate back into place.
5. On S5 modules with locking knob, push the knob in and turn it so that the knob slot is vertical.

Figure A-2 shows how to insert an S5 module into the adapter casing.

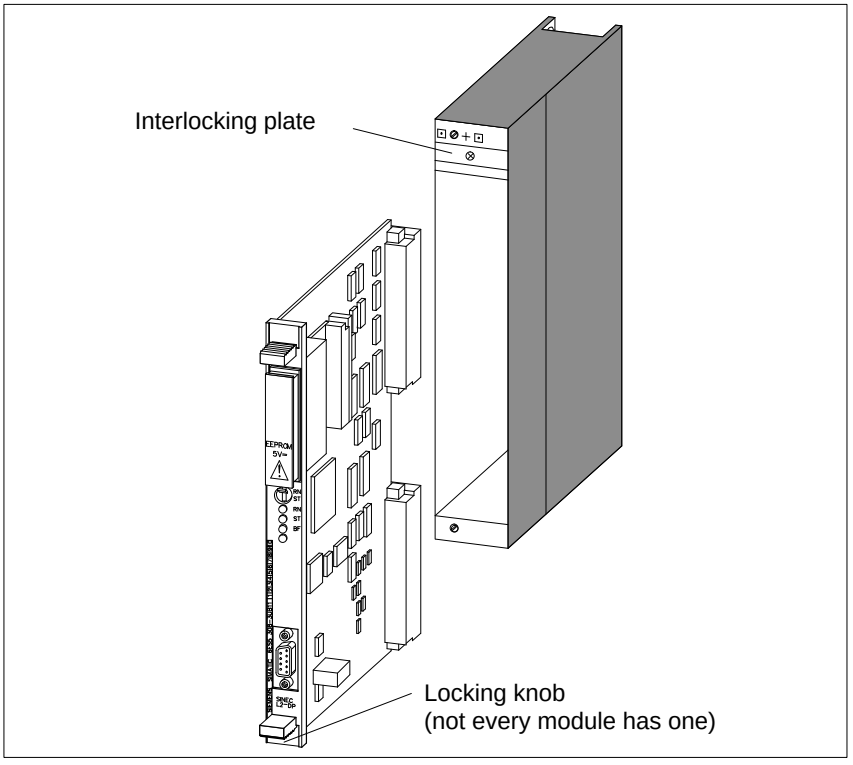


Bild A-2 Inserting an S5 Module into the Adapter Casing

A.4 Interrupt Processing

Introductory Remarks

The adapter casing converts S5 interrupts into S7 interrupt functions and interrupt signals.

Interrupt Routing

All of the S5 module's interrupts are forwarded as (S7) process interrupts. The interrupts are routed as follows:

S5 Interrupt Circuit	S7 Interrupt Circuit
/INT A	/I1
/INT B	/I2
/INT C	/I3
/INT D	/I4

Interrupt During Active OD

No new interrupts are generated while OD (OUTPUT DISABLE) is active (for instance when the CPU is at STOP). Interrupts which were already pending are serviced. The falling edge of the OD signal resets the S7-specific interrupt functions.

Whether or not the S7-specific interrupt functions are reset with the falling edge of the OD signal depends on the S5 module (please refer to the relevant manuals). In the case of S5 modules in which the falling edge of the OD signal does not reset an interrupt, a new interrupt is subsequently generated.

Ascertaining the Interrupt-Generating Module

When an S5 module in the adapter casing generates an interrupt, the logical address of that module in entered in the interrupt OB's local data area.

Acknowledging an Interrupt

An interrupt is acknowledged in the usual manner, that is, the same as in S5 systems (refer to the Manual or the Product Information for details). The CPU automatically carries out the S7-specific additional interrupt functions.

A.5 Technical Specifications

Dimensions and Weight	
Dimensions W × H × D	50mm × 290mm × 210 mm (1.96 in. x 11.41 in. x 8.26 in.)
Weight	Approx. 300 g
Voltages and Currents	
System voltage [1]	5 V DC
• Rated voltage	5.1 V DC
• Range	4.75 V to 5.25 V DC
Auxiliary voltage [1]	
• Rated voltage	24 V DC
• Range	18 V to 32 V DC
Battery voltage [1]	
• Rated voltage	3.4 V DC
• Range	2.75 V to 4.4 V DC

Maximum Current Carrying Capacity	
The maximum power which may be drawn from the adapter casing is as follows:	
• From the system voltage	3 A
• From the auxiliary voltage	0.5 A
• From the battery voltage	0.5 mA

[1] Is looped through from the S7-400 power supply

Addressing S5 Modules (Adapter Casing and IM 463-2)

B

In this Chapter

This chapter describes

- how to address S5 modules inserted in the adapter casing, and
- how to address S5 modules connected via the IM 463-2.

B.1 Addressing S5 Modules

Introductory Remarks

There are two ways of using an IP xxx S5 module in the S7-400:

- By installing it in the adapter casing in the S7 central rack
- By using an S5 expansion rack and connecting the S5 module via the IM 463-2 interface module in the S7 central rack and the IM 314 interface module in the S5 expansion rack.

Addressing

In order to be able to address an S5 module in the S7-400, you must set addresses in two different places:

- The address under which the module is to be referenced in the user program and the address set on the module must be entered in STEP 7.
- The address of the S5 module in a permissible S5 address space (address switch on the module).

S7 Address

The address under which the module is to be referenced in the S7-400 must be set under STEP 7. It is not possible to use default addresses.

Proceed as follows for an S5 module in the S7-400:

– S7 address:	Logical address. The value range depends on the CPU.
– S5 address:	Address set on the module. Value range from 0 to 255.
– Length:	Size of the address block. Value range from 0 to 128 (in bytes).
– Process image subarea:	Process image subarea specification. Value range: 0 (entire process image) 1 to 8 (process image subarea)
– Area:	Value range P, Q, IM3, IM4.

S5 Address Areas

S5 modules in the S7-400 may be addressed in the following addressing areas:

- I/O area (P area)
- Extended I/O area (Q, IM3, IM4)
- Page area

I/O Area

A PESP signal (that is, a memory I/O select signal) is generated in the P area only when S5 modules are interfaced to the system via the adapter casing. The signal is forwarded to the S5 module. No PESP signal is generated for the Q, IM3 or IM4 areas.

When the S5 modules are interfaced via the IM 463-2, the PESP signal is generated by the IM 314 in the S5 expansion unit (for the selected P, Q, IM3 or IM4 area).

This corresponds to the 256-byte I/O area as defined for SIMATIC S5. The S5 address of the module in these areas is set on the module using jumpers or switches. Please refer to the relevant manual for the correct setting.

For modules which reserve input and output areas, an entry must be made under STEP 7 for each area.

Page Area

In order to operate an S5 module with page addressing, you need the revised standard function blocks (S7 functions). These standard function blocks call special system functions which emulate the S5 page commands. These standard function blocks can be linked into your application program.

Even in the case of page addressing, you must assign a logical address. This logical address is entered in the interrupt OB's local data area as start information.

Under STEP 7, you must assign an S7 address and an S5 address in the input area with length 0. You may not assign an address for this module in the output area.

Note

When using S5 modules in your S7-400, you must observe the following carefully when setting the module addresses:

- No two S7 addresses may be the same.
- No two S5 addresses may be the same in any given area (P, Q, IM3, IM4).
- Even when an S5 module has an address area with a length of 0, its address may not lie within the address area of another S5 module.

Example of Addressing in the Page Area

The CPU and an IP (an IP being an intelligent I/O module) interchange data via the S5 bus interface and a 2 Kbyte dual-port RAM which is divided into two “pages”.

The addressing area in which the pages are located is set at the factory. You need only set the page number for the first page on the module.

A module’s two pages always reserve two consecutive numbers. The IP thus knows the address for the second page automatically.

The same addressing area is set for page addressing on each module at the factory.

When you configure your hardware with STEP 7, you must enter the following parameters in the input area:

- S7 address: Logical address
- S5 address: 0 (value range from 0 to 255, may not appear more than once in the specified area)
- Length: 0
- Process image subarea: 0
- Area: P (value range P, Q, IM3, IM4)

Example for Addressing in the P Area

An IPxxx requires 32 addresses in order to pass the required parameters. Only the start address of the module need be set. The next 31 addresses are reserved by an internal decoding procedure, and are then no longer available for other modules. The addresses can be set in increments of 32.

A module’s input and output addresses (S5 and S7) must be identical. This is a prerequisite which must be observed to ensure proper use of the standard function blocks.

When you configure your hardware with STEP 7, you must enter the following parameters in the input and output areas:

- S7 address: Must be a logical address equal to or greater than 512 (which you can use in your application program to reference the module)
- S5 address: Same as on the module
- Length: 32 bytes
- Process image subarea: 0
- Area: Depends on the area set on the module or IM 314 (P, Q, IM3 or IM4)

The address of the IP 244 may not lie within the process image. There are two ways to ensure this:

- Set an S7 address equal to or greater than 512
- Select a process image subarea value equal to or greater than 0

The IP 240 Counter, Position Decoder and Positioning Module

C

In this Chapter

This chapter describes the counting, position decoding and positioning functions for the IP 240 module, lists their technical specifications and the assignment of the required data blocks, and provides programming examples to show you how to use the functions.

Chapter Overview

C.1 Overview

Introductory Remarks

This addendum supplements Chapters 7, 8 and 10 of the Manual. It describes the standard functions of the IP 240 counter, position decoder and positioning module for the SIMATIC S7-400.

The IP 240 counter, position decoder and positioning module can be connected via the adapter casing in a SIMATIC S7-400 programmable controller or via the IM 463-2 and IM 314 interface modules in a 185U expansion rack.

For this purpose, there are new standard functions which can execute in the S7-400 programmable controller's CPUs.

Standard Software

The standard functions are provided in the form of a SETUP on a diskette. The SETUP can execute only under Windows 95.

When the SETUP executes, it creates a library containing only the standard functions for the IP 240, and a programming example.

An on-line Help facility is provided for the standard functions.

Prerequisite for Initializing the Module

Before initializing the IP 240, you should make sure that the following prerequisite has been fulfilled:

- Be sure that Version 2.0 or a newer version of STEP 7 has been correctly installed on your programming device or PC.

Installation

All the software (standard functions and examples) can be found on the two 3.5 inch diskettes "Counting and Position Decoding" (FIP240Z) and "Positioning" (FIP240P).

Here's how to install the software:

1. Insert the diskette in your programming device or PC diskette drive.
2. Under Windows 95, start the dialog for installing software by double-clicking on the ***Software*** symbol in ***Control panel***.
3. Select the diskette drive and the ***SETUP.EXE*** file and start the installation procedure.
4. Follow the step-by-step directives displayed by the installation program.

Result:

The software is installed in the following directories on the target drive:

Software	Directory
Counting and position decoding:	
• Standard functions:	STEP7_V2\S7LIBS\IP240ZLI
• Examples:	STEP7_V2\EXAMPLES\IP240WEX STEP7_V2\EXAMPLES\IP240ZEX
Positioning:	
• Standard functions:	STEP7_V2\S7LIBS\IP240PLI
• Example:	STEP7_V2\EXAMPLES\IP240PEX

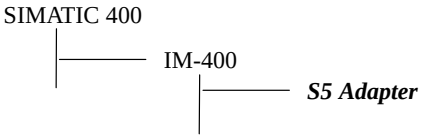
Note

If you selected a directory other than STEP 7_V2 when you installed STEP 7, that directory will be entered.

Configuring

Before you can configure your system, you must have created a project in which you can store the parameters. You can find additional information on module configuring in your *Standard Software for S7 and M7, STEP 7* User Manual. Only the most important steps are described below.

1. Start the SIMATIC Manager and call the configuration table in your project.
2. Select a rack and place it at the desired position.
3. Open the rack.
4. Select the following components in the hardware catalog:



Please take all other information needed to configure the hardware from the chapter “Addressing S5 Modules (Adapter Casing and IM 463-2)”.

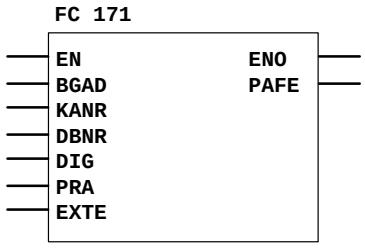
C.2 Counting Functions

Function FC 171 (STRU_DOS)

Introductory Remarks

The call, meaning and parameter values for the FC 171 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL
	CALL FC 171 (BGAD := , KANR := , DBNR := , DIG := , PRA := , EXTE := , PAFE :=);

Parameters

The table below provides an overview of the parameters required by the FC 171 function.

Name	Parameter Type	Data Type	Description
BGAD	INPUT	INT	Module address
KANR	INPUT	INT	Channel number
DBNR	INPUT	INT	Data block number
DIG	INPUT	WORD	Assign digital output
PRA	INPUT	WORD	Assign interrupts
EXTE	INPUT	WORD	Control counter enable
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

- DBNR: INT = x
  x: Dependent on the CPU used (number 0 is not permitted)
- EXTE: WORD
  corresponds to the EXT parameter in S5 (had to be renamed because EXT is a compiler code word).

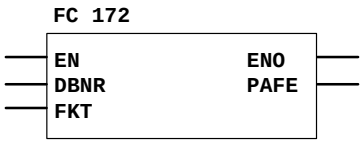
For all other parameter values, please refer to the Manual (Section 8.3.1, “Configuring Function Block“).

Function FC 172 (STEU_DOS)

Introductory Remarks

The call, meaning and parameter values for the FC 172 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL
	CALL FC 172 (DBNR := , FKT := , PAFE :=);

Parameters

The table below provides an overview of the parameters required by the FC 172 function.

Name	Parameter Type	Data Type	Description
DBNR	INPUT	INT	Data block number
FKT	INPUT	INT	Function number
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

DBNR: INT = x
x: Dependent on the CPU used (number 0 is not permitted)

For the values of the remaining parameters, please refer to the Manual (Section 8.3.2, “Control Function Block”).

Technical Specifications FC 171 and FC 172

The technical specifications for FC 171 and FC 172 are listed below:

	FC 171	FC 172
Block number	171	172
Block name	STRU_DOS	STEU_DOS
Version	1.0	1.0
Space reserved in load memory	2.148 bytes	1.628 bytes
Space reserved in work memory	1.830 bytes	1.354 bytes
Space reserved in data area	Data block specified in *DBNR* parameter	
Space reserved in local data area	24 bytes	10 bytes
System functions called	SFC 24 TEST_DB SFC 36 MSK_FLT SFC 37 DMSK_FLT SFC 38 READ_ERR SFC 47 WAIT	SFC 41 DIS_AIRT SFC 42 EN_AIRT SFC 47 WAIT

Processing Times

The processing times shown below apply for the CPU 416-1.

Module	Function	Processing Time
FC 171		12.2 ms
FC 172	Function 1	2.2 ms
	Function 2	2.0 ms
	Function 3	2.2 ms
	Function 4	2.3 ms

C.3 Position Decoding Functions

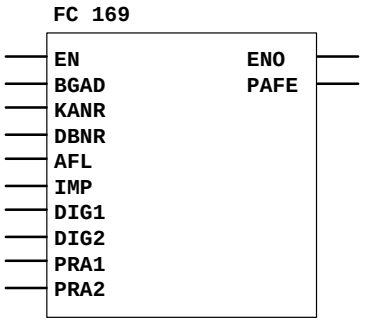
Function FC 164 (STRU_WEG)

Introductory Remarks

The call, meaning and parameter values for the FC 169 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL

	`CALL FC 169 (`
	`BGAD :=  ,`
	`KANR :=  ,`
	`DBNR :=  ,`
	`AFL  :=  ,`
	`IMP  :=  ,`
	`DIG1 :=  ,`
	`DIG2 :=  ,`
	`PRA1 :=  ,`
	`PRA2 :=  ,`
	`PAFE :=  );`

Parameters

The table below provides an overview of the parameters required by the FC 169 function.

Name	Parameter Type	Data Type	Description
BGAD	INPUT	INT	Module address
KANR	INPUT	INT	Channel number
DBNR	INPUT	INT	Data block number
AFL	INPUT	INT	Resolution for sensor pulses
IMP	INPUT	INT	Set zero mark monitoring
DIG1	INPUT	WORD	Assign digital output D1
DIG2	INPUT	WORD	Assign digital output D2
PRA1	INPUT	WORD	Assign interrupts
PRA2	INPUT	WORD	Assign interrupts
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

DBNR: INT = x

x: Dependent on the CPU used (0 is not permitted)

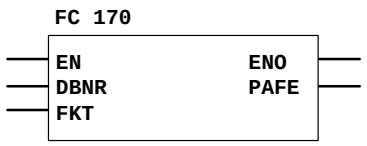
For the values of the remaining parameters, please refer to the Manual (Section 7.3.1, “Configuring Function Block”)

Function FC 170 (STEU_WEG)

Introductory Remarks

The call, meaning, and parameter values for the FC 165 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL
	CALL FC 170 (DBNR := , FKT := , PAFE :=);

Parameters

The table below provides an overview of the parameters required by the FC 170 function.

Name	Parameter Type	Data Type	Description
DBNR	INPUT	INT	Data block number
FKT	INPUT	INT	Function number
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

DBNR: INT = x
x: Dependent on the CPU used (0 is not permitted)

For the values of all other parameters, please refer to the Manual (Section 7.3.2, “Control Function Block“)

Technical Specifications for FC 169 and FC 170

The technical specifications for FC 169 and FC 170 are listed below:

	FC 169	FC 170
Block number	169	170
Block name	STRU_WEG	STEU_WEG
Version	1.0	1.0
Space reserved in load memory	2.724 bytes	2.378 bytes
Space reserved in work memory	2.348 bytes	2.028 bytes
Space reserved in data area	Data block specified in the *DBNR* parameter.	
Space reserved in local data area	26 bytes	12 bytes
System functions called	SFC 24 TEST_DB SFC 36 MSK_FLT SFC 37 DMSK_FLT SFC 38 READ_ERR SFC 47 WAIT	SFC 41 DIS_AIRT SFC 42 EN_AIRT SFC 47 WAIT

Processing Times

The specified processing times apply for the CPU 416-1.

Block	Function	Processing Time
FC 169	No track transferred	9.7 ms
	All tracks transferred	10.0 ms
FC 170	Function 1	2.5 ms
	Function 2	2.1 ms
	Function 3	2.1 ms
	Function 4 no track all tracks	 3.4 ms 3.8 ms
	Function 5	2.2 ms

C.4 Positioning Functions

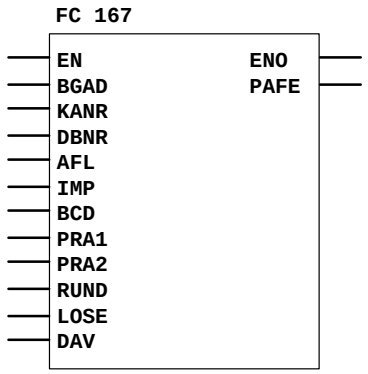
Function FC 167 (STRU_POS)

Introductory Remarks

The call, meaning, and parameter values for the FC 167 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL

	`CALL FC 167 (`
	`BGAD :=  ,`
	`KANR :=  ,`
	`DBNR :=  ,`
	`AFL  :=  ,`
	`IMP  :=  ,`
	`BCD  :=  ,`
	`PRA1 :=  ,`
	`PRA2 :=  ,`
	`RUND :=  ,`
	`LOSE :=  ,`
	`DAV  :=  ,`
	`PAFE :=  );`

Parameters

The table below provides an overview of the parameters required by the FC 165 function.

Name	Parameter Type	Data Type	Description
BGAD	INPUT	INT	Module address
KANR	INPUT	INT	Channel number
DBNR	INPUT	INT	Data block number
AFL	INPUT	INT	Resolution for sensor pulses
IMP	INPUT	INT	Set zero mark monitoring
BCD	INPUT	WORD	Select number formats
PRA1	INPUT	WORD	Assign interrupts
PRA2	INPUT	WORD	Assign interrupts
RUND	INPUT	INT	Select axis type
LOSE	INPUT	INT	Compensation of slackness in gear
DAV	INPUT	INT	Select switching performance of IP outputs
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

DBNR: INT = x
x = Depends on the CPU used (0 is not permitted)

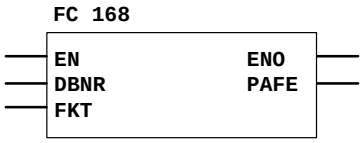
For the values of all other parameters, please refer to the Manual (Section 10.23.2, ““Configuring Function Block””)

Function FC 168 (STEU_POS)

Introductory Remarks

The call, meaning and parameter value for the FC 168 function are described below.

Calling the Function

Ladder Diagram LAD	Statement List STL
	CALL FC 168 (DBNR := , FKT := , PAFE :=);

Parameters

The table below provides an overview of the parameters required by the FC 168 function.

Name	Parameter Type	Data Type	Description
DBNR	INPUT	INT	Data block number
FKT	INPUT	WORD	Function number
PAFE	OUTPUT	BYTE	Error flag byte

Parameter Values

DBNR: INT = x
x: Dependent on the CPU used (number 0 is not permitted)

For the values of the remaining parameters, please refer to the Manual (Section 10.23.3, “Control Function Block ”)

Technical Specifications FC 167 and FC 168

The technical specifications for FC 167 and FC 168 are listed below:

	FC 167	FC 168
Block number	167	168
Block name	STRU_POS	STEU_POS
Version	1.0	1.0
Space reserved in load memory	2.890 bytes	2.118 bytes
Space reserved in work memory	2.494 bytes	1.782 bytes
Space reserved in data area	Data block specified in *DBNR* parameter. The data assigned depends on the number of stored positions.	
Space in local data area	24 bytes	12 bytes
System functions called	SFC 24 TEST_DB SFC 36 MSK_FLT SFC 37 DMSK_FLT SFC 38 READ_ERR SFC 47 WAIT	SFC 41 DIS_AIRT SFC 42 EN_AIRT SFC 47 WAIT

Processing Times

The processing times shown below apply for the CPU 416–1.

Module	Function	Processing Time
FC 167		14.8 to 130.2 ms The processing time depends on the number of positions to be transferred (0 to 254)
FC 168	Function 1	2.2 ms
	Function 20	2.1 ms
	Function 21	2.2 ms
	Function 22	2.6 ms
	Function 3	2.3 ms
	Function 41/42	up to 2.9 ms
	Function 5	2.4 ms
	Function 6	3.3 ms

C.5 Differences between SIMATIC S7 and SIMATIC S5

Memory Locations of the Data Addresses

As a rule, the following applies for SIMATIC S7: The memory locations of the data addresses are counted **byte by byte**. The location of an S5 data word (DW n) corresponds to the location DBW (2*n) of the S7 data word.

Format of the Data Blocks

The format of the data blocks has been largely retained. The following points distinguish S7 from S5 (for all modes):

- With S7, the returned data block number is located in the data word DBW 48 (the number can be greater than one byte). The data byte DBB 47 occupied by the data word number in S5 is occupied by the standard functions and is therefore no longer available.
- The basic address of the module is returned in the data word DBW 42.

C.6 Programming Example for “Counting” Mode

Prerequisites, Settings, Blocks and Addresses

Overview

The programming example describes the standard functions for operating the IP 240 counter, position decoding and positioner module in “Counting” mode.

Objectives of the programming example:

- The example should show the most important functions in exemplary form.
- It should enable testing of the hardware (such as sensors) for functionability.
- The example is therefore simple and easy to follow.
- And it can be expanded if desired without a great deal of overhead.

The example shows how to parameterize the module at start-up, the count process with software and hardware gates, how to transfer a new count starting value, and how an interrupt is generated at zero crossing.

The example can be implemented with only a minimum hardware complement (1 byte for inputs, 1 byte for outputs). Essentially, it uses the functions “Monitor/Modify variable”.

Device Configuration

The devices listed below are only some of those which can be used to try out the sample program:

- An S7–400 programmable controller system (rack, power supply unit, CPU)
- An adapter casing
- An IP 240 module with suitable sensor
- One digital input and one digital output module
- A programming device (such as a PG 740)

It is possible to do without both the digital input module and the digital output module when all functions are executed with “Monitor/Modify variable”. This would require changes in organization block OB 1.

As sensors for the IP 240 module, one contact is connected to the CLK terminal as the count contact, and one to the GT terminal as the gate contact.

The module must have a voltage supply of 24 V (X6 connector)

Settings in the CPU

You must set the addresses for the adapter casing via STEP 7 (hardware configuration). In the example, the following I/O settings have been assumed:

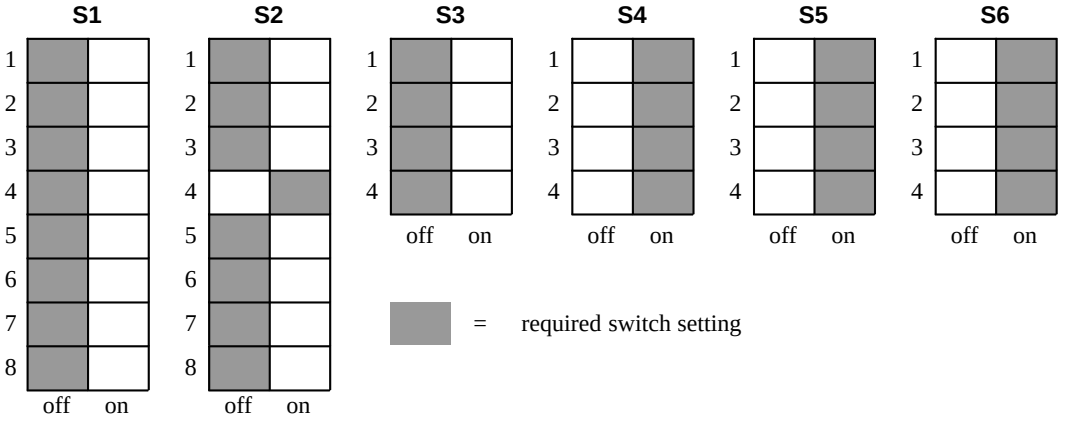
- S7 address: 512,
- S5 address: 0 (I/O area: P)
- Length: 16 bytes,
- Process image subtable: 0.

The following interrupt settings are required in the CPU:

- Process interrupt: OB 40,
- Interrupt: I1 (S5 assignment: IA)

Settings on the IP 240

"Counting" mode:



- S1: No process interrupts via IB 0
- S2: Interrupt circuit A, I/O area P
- S3: I/O address 0
- S4: Sensor signals asymmetrical
- S5: Sensor signals +24 V (channel 1)
- S6: Sensor signals + 24 V (channel 2)

Blocks

For the programming example, the data block DB 172 "C_data" is used. It has the same format as the corresponding standard data block. The data necessary for the example has also been entered.

The following blocks are used:

Block	Name	Purpose
OB 1	Cycle	Cyclic program processing
OB 40	Interrupt	Interrupt processing
OB 100	Start-up	Start-up processing for restart
DB 172	C_data	Data block for counting
FC 171	STRU_DOS	Configuring block
FC 172	STEU_DOS	Control block

Addresses

The inputs and outputs are mapped onto memory bits at the beginning and end of OB 1. Within the test program, only the memory bits are used.

Signal	Memory Bit	Description
I 3.0	M 170.0	Start/stop counting
I 3.1	M 170.1	Write count starting value
I 3.2	M 170.2	Disable/enable interrupts
I 3.3	M 170.3	Delete interrupt display
I 3.4	–	Unassigned
I 3.5	–	Unassigned
I 3.6	–	Unassigned
I 3.7	–	Unassigned

Signal	Memory Bit	Description
Q 3.0	M 171.0	Counting has been enabled
Q 3.1	M 171.1	–
Q 3.2	M 171.2	Interrupts have been enabled
Q 3.3	M 171.3	Interrupt marker
Q 3.4	–	Unassigned
Q 3.5	–	Unassigned
Q 3.6	–	Unassigned
Q 3.7	M 171.7	Error has occurred

The following memory areas are also occupied:

Bit Memory Address Area	Description
MB 172	Edge memory bit
MB 173	Error memory bit
MB 174 to MB 179	Error bytes of the PAFE parameter

Start-up Program and Error Responses

Start-up Program

The start-up program is located in OB 100. When OB 100 has been processed, you can check the following entries with “Monitor/Modify variable”:

- DB 172.DBB 2 to DBB 7: Product code of the module
- DB 172.DBB 8 to DBB 13: Firmware version
- DB 172.DBB 14 and DBB 15: Hardware version
- DB 172.DBB 46: B#16#02 (“Counting” mode)
- DB 172.DBW 48: Data block number
- DB 172.DBW 52: Basic address of the module

The actual value

- DB 172.DBD 60: (BCD-coded) or
- DB 172.DBD 64: (binary-coded)

is the count starting value, which is transferred to the module when the data block is started up.

If all inputs show the signal state ‘0’, no output may be activated.

Responses to errors

If an error or fault occurs during execution of the start-up program, the cyclic block calls are no longer processed; the error memory bit.

After every block call in the cyclic program, an error memory bit is set when an error occurs (BR = ‘0’), which in turn causes the group error message to be signalled at output Q3.7 (M 171.7).

In the case of a group error message, the associated error bit indicates which block call has caused the error. A precise description of the error can be found in the corresponding PAFE byte and in the error words of the data block (see the IP 240 Manual, Sections 8.3.1 “Configuring Function Block” and 8.3.2 “Control Function Block“).

Cyclic Program

General Remarks

The cyclic program is located in OB 1.

At the beginning of the program, the inputs are mapped to memory bits which are then used in the rest of the program. At the end of the program, control memory bits are transferred to the outputs and displayed.

Reading the Actual Value, End Value and Status Bits

The FC 172 function is called absolutely with the function 1; this means that it is **always** processed and reads the actual value, the end value and the status bits in every program cycle.

The end value is not calculated until the first count process has been completed (see below).

Starting and Stopping Counting

With positive edge at input I 3.0 (M 170.0), the control bit STRT is set and the FC 172 function is called with function 2 (write control bits). Now the IP 240 records the count pulses: the actual value is counted downward, beginning at the count starting value which was preset at start-up. The released counting is displayed at output Q3.0 (M 171.0).

With negative edge at input I 3.0 (M 170.0), the control bit STRT is reset and written to the module. Now the counting is completed: the actual value reached is stored as the end value. When the count process is started again, the counting begins again at the count starting value.

Counting with the Hardware Gate

The count process was previously influenced by the software through the control bit STRT. You can also influence the count process with the gate contact by specifying the value W#16#0001 as the EXTE parameter of the FC 171 function during structuring and restart the CPU.

The count process with hardware gate is executed in the same way as the one previously described.

Transferring the Count Starting Value

With positive edge at input I 3.0 (M 170.1), you can specify a new count starting value. Set the count starting value to the number you require in the data block DB 172.DBD 68 (for example, with “Monitor/Modify variable”) and activate the input.

The new count starting value is transferred to the module (call FC 172 with function 4) and comes into effect the next time a count process is started.

Interrupt Program

Interrupt Block

The interrupt program is located in the organization block OB 40.

Enabling Interrupts

In the start-up program, the module is structured such that when the actual value passes through zero (PRA = W#16#0001) an interrupt is generated. Interrupt generation is initially blocked (control bit AMSK = ‘1’).

In the cyclic program, positive edge at input I 3.2 (M 170.2) causes the control bit AMSK to be reset and transferred to the module (FC 172 with function 2). Now an interrupt is generated when the actual value crosses zero. The enable of interrupt generation is signalled at output Q 3.2 (M 171.2).

The interrupt enable is canceled through transfer of the control bit AMSK to the module with negative edge at input I 3.2 (M 170.2).

Acknowledging Interrupts

In the interrupt program, the FC 172 function is called by means of function 3 (read interrupt request bytes). The interrupt request bytes are transferred from the module to the data block. These contain the cause of the interrupt (for example, interrupt generation at zero crossing on channel 1: DB 172.DBX 40.0 is set). When an interrupt is generated in this way, the memory bit M 71.3 is set, which then causes the interrupt to be signalled via output Q 3.3 in the cyclic program.

In the cyclic program you can delete the interrupt display again with positive edge at input I 3.3 (M 171.3).

C.7 Programming Example for “Position Decoding” Mode

Prerequisites, Settings, Blocks and Addresses

Overview

The programming example describes the standard functions for operating the IP 240 counter, position decoder and positioning module in “Position decoding” mode.

Objectives of the programming example:

- The example should show the most important functions in exemplary form.
- It should enable testing of the hardware (such as sensors) for functionability.
- The example is therefore simple and easy to follow.
- And it can be expanded if desired without a great deal of overhead.

The example shows how to parameterize the module at start-up, how to force the reference bits and the digital outputs via the tracks, how to preset new track limits and zero displacement, and how an interrupt is generated when a track is reached.
The example can be realized with only a minimum hardware complement (1 byte for inputs, 1 byte for outputs). Essentially, it uses “Monitor/Modify variable”.

Device Configuration

The devices listed below are only some of those which can be used to try out the sample program:

- An S7-400 programmable controller system (rack, power supply unit, CPU)
- An adapter casing
- An IP 240 module with suitable sensor
- One digital input and one digital output module
- A programming device (such as a PG 740)

It is possible to do without both the digital input module and the digital output module when all functions are executed with “Monitor/Modify variable”. This would require changes in organization block OB 1.

As sensor for the IP 240 module, an angular encoder is connected to channel 1 of the module.

The module must have a voltage supply of 24 V (X6 connector)

Settings in the CPU

You must set the addresses for the adapter casing via STEP 7 (hardware configuration). The following I/O settings have been assumed:

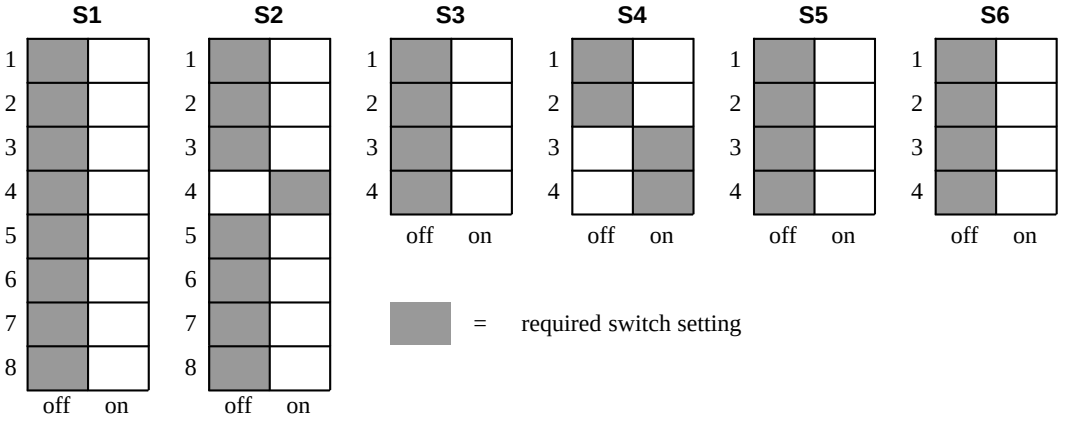
- S7 address: 512,
- S5 address: 0 (I/O area: P)
- Length: 16 bytes
- Process image subtable: 0.

The following interrupt settings are required in the CPU:

- Process interrupt: OB 40,
- Interrupt I1 (S5 assignment: IA).

Settings on the IP 240

"Position decoding" mode:



- S1: No process interrupts via IB 0
- S2: Interrupt circuit A, I/O area P
- S3: I/O address 0
- S4: Sensor signals symmetrical
- S5: Sensor signals +5 V (channel 1)
- S6: Sensor signals + 5 V (channel 2)

Blocks

For the programming example, the data block DB 170 "PD_data" is used. It has the same format as the corresponding standard data block. The data necessary for the example has also been entered.

The following blocks are used:

Block	Name	Purpose
OB 1	Cycle	Cyclic program scanning
OB 40	Interrupt	Interrupt processing
OB 100	Start-up	Cold restart processing
DB 170	PD_data	Data block for position decoding
FC 169	STRU_WEG	Structure block
FC 170	STEU_WEG	Control block

Addresses

The inputs and outputs are mapped onto memory bits at the beginning and end of OB 1. Within the test program, only the memory bits are used.

Signal	Memory Bit	Description
I 2.0	M 180.0	Write track limits
I 2.1	M 180.1	Write zero displacement
I 2.2	M 180.2	Disable/enable interrupts
I 2.3	M 180.3	Delete interrupt display
I 2.4	–	Unassigned
I 2.5	–	Unassigned
I 2.6	–	Unassigned
I 2.7	–	Unassigned

Signal	Memory Bit	Description
Q 2.0	M 181.0	Write track limits
Q 2.1	M 181.1	–
Q 2.2	M 181.2	Interrupts have been enabled
Q 2.3	M 181.3	Interrupt display
Q 2.4	–	Unassigned
Q 2.5	–	Unassigned
Q 2.6	–	Unassigned
Q 2.7	M 181.7	Error has occurred

The following memory areas are also occupied:

Bit Memory Address Area	Description
MB 182	Edge memory bit
MB 182	Error memory bit
MB 184 bis MB 189	Error bytes of the PAFE parameter

Start-up Program and Error Responses

Start-up Program

The start-up program is in OB 100. When OB 100 has been processed, you can check the following entries with “Monitor/Modify variable”:

- DB 170.DBB 2 to DBB 7: Product code of the module
- DB 170.DBB 8 to DBB 13: Firmware version
- DB 170.DBB 14 and DBB 15: Hardware version
- DB 170.DBB 46: B#16#01 (“Position decoding” mode)
- DB 170.DBW 48: Data block number
- DB 170.DBW 52: Basic address of the module

The actual value

- DB 170.DBD 60: (BCD-coded) or
- DB 170.DBD 64: (binary-coded)

is zero.

If all inputs show the signal state ‘0’, no output may be activated.

Responses to Errors

If an error or fault occurs during execution of the start-up program, the cyclic block calls are no longer processed; the error memory bit is set.

After every block call in the cyclic program, an error is flagged when an error occurs (BR = ‘0’), which in turn causes a group error message to be output at Q 2.7 (M 181.7).

In the case of a group error message, the associated error bit indicates which block call has caused the error. A precise description of the error can be found in the corresponding PAFE byte and in the error words of the data block (see the IP 240 Manual, Sections 7.3.1 “Configuring Function Block” and 7.3.2 “Control Function Block”).

Cyclic Program

General Remarks

The cyclic program is in OB 1.

At the beginning of the program, the inputs are mapped to memory bits which are then used in the rest of the program. At the end of the program, the control memory bits are transferred to the outputs and displayed.

Reading the Actual Value and Status Bits

The FC 170 function is called absolutely with function 1; this means that it is **always** processed and reads the actual value and the status bits in every program cycle.

Setting the Reference Bits

The actual value changes according to the sensor pulses. If the actual value runs into a configured track, the reference bit REFx belonging to the track is set. This can be monitored with “Monitor/Modify variable”.

- DB 170.DBD 60 Actual value
- DB 170.DBX 39.0 Sign of the actual value
- DB 170.DBX 38.0 REF1,
- DB 170.DBX 38.2 REF3.

The hysteresis is not taken into account when the reference bits are set.

Writing New Track Limits

You can define new limit values for the tracks that were configured at start-up. Change the track limits in the data block

- DB 170.DBD 68 Start value, track 1
- DB 170.DBD 72 End value, track 1
- DB 170.DBD 84 Start value, track 3
- DB 170.DBD 88 End value, track 3

and transfer the values with the input I 2.0 (M 180.0). Now the reference bits are controlled according to the new track limits.

Writing Zero Displacement

To change the zero displacement, set the desired value in the data block

- DB 170.DBD 132 Zero displacement

and transfer the zero displacement with the input I 2.1 (M 180.1). The zero displacement is added to the current actual value (a negative value can also be specified).

Setting Digital Outputs

The LEDs in the front panel allow you to observe the setting of the digital outputs D1 and D2 on the module.

With the DIG1 and DIG2 parameters of FC 169, you determine at what point the module is to set the digital outputs. The digital outputs are released through the control bits:

- DB 170.DBX 34.0 DA1S = TRUE,
- DB 170.DBX 34.1 DA1F = FALSE,
- DB 170.DBX 34.2 DA2S = TRUE,
- DB 170.DBX 34.3 DA2F = FALSE.

You can use the input I 2.3 (M 180.3) to transfer the control bits (this input actually enables the interrupts, but if you deactivate it again immediately, the control bits will be transferred with the interrupts still disabled).

If the actual value now runs into a configured track, the digital outputs will be set (D1 with track 1 and D2 with track 3). When the value leaves the track via the same limit as when it entered it (change of direction within a track), the hysteresis is taken into account when the digital outputs are deactivated.

You set the hysteresis

- DB 170.DBB 45 Hysteresis

during start-up with FC 169.

Interrupt Program

Interrupt Block

The interrupt program is located in the organization block OB 40.

Enabling Interrupts

In the start-up program, the module is structured such that when tracks 1 or 3 are reached (PRA = W#16#0005) an interrupt is generated. Interrupt generation is initially blocked (control bit AMSK = ‘1’).

In the cyclic program, a positive edge at input I 2.2 (M 180.2) causes the control bit AMSK to be reset and transferred to the module (FC 170 with function 2). Now an interrupt is generated when one of the tracks 1 and 3 is reached. The enable of interrupt generation is signalled at output Q 2.2 (M 181.2).

The interrupt enable is canceled through transfer of the control bit AMSK to the module with negative edge at input I 2.2 (M 180.2).

Acknowledging Interrupts

In the interrupt program, the FC 170 function is called by means of function 3 (read interrupt request bytes). The interrupt request bytes are transferred from the module to the data block. These contain the cause of the interrupt (for example, interrupt generation when track 1 is reached: DB 170.DBX 40.0 is set). When an interrupt is generated in this way, the memory bit M 181.3 is set, which then causes the interrupt to be signalled via output Q 2.3 in the cyclic program.

In the cyclic program you can delete the interrupt display again with positive edge at input I 2.3 (M 181.3).

C.8 Programming Example for “Positioning” Mode

Prerequisites, Settings, Blocks and Addresses

Overview

The programming example describes the standard functions for operating the IP 240 counter, position decoder and positioning module in “Positioning” mode.

Objectives of the programming example:

- The example should show the most important functions in exemplary form.
- It should enable testing of the hardware (such as sensors) for functionability.
- The example is therefore simple and easy to follow.
- And it can be expanded if desired without a great deal of overhead.

The example shows how to parameterize the module at start-up, how to read the actual value, dynamic specification of a function (software synchronization, approaching a new position, new clearance values etc.) and how an interrupt is generated when a clearance value is reached.
The example can be realized with only a minimum hardware complement (1 byte for inputs, 1 byte for outputs). Essentially, it uses “Monitor/Modify variable”.

Device Configuration

The devices listed below are only some of those which can be used to try out the sample program:

- An S7-400 programmable controller system (rack, power supply unit, CPU)
- An adapter casing
- An IP 240 module with suitable sensor
- One digital input and one digital output module
- A programming device (such as a PG 740)

It is possible to do without both the digital input module and the digital output module when all functions are executed with “Monitor/Modify variable”. This would require changes in organization block OB 1.

As sensor for the IP 240 module, an angular encoder is connected to channel 1 of the module.

The module must have a voltage supply of 24 V (X6 connector)

Settings in the CPU

You must set the addresses for the adapter casing via STEP 7 (hardware configuration). The following I/O settings have been assumed:

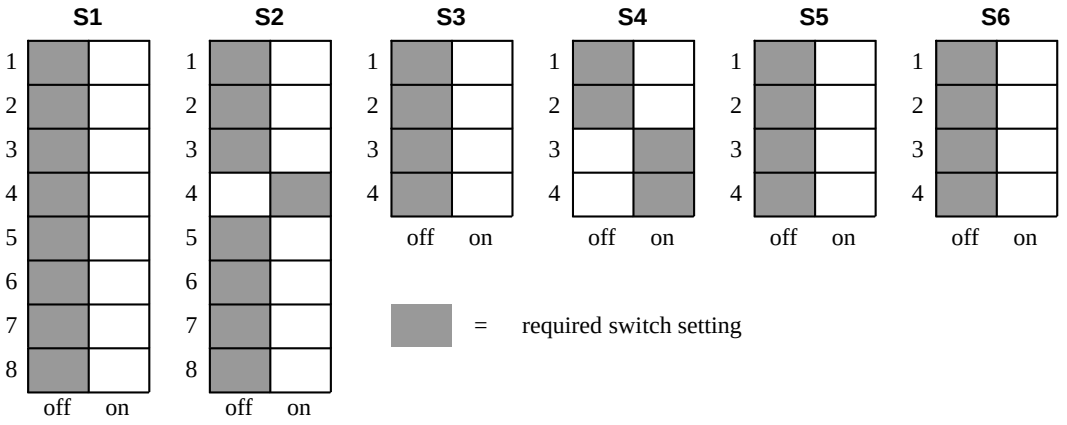
- S7 address: 512,
- S5 address: 0 (I/O area: P)
- Length: 16 bytes
- Process image subtable: 0.

The following interrupt settings are required in the CPU:

- Process interrupt: OB 40,
- Interrupt I1 (S5 assignment: IA).

Settings on the IP 240

"Positioning" mode:



- S1: No process interrupts via IB 0
- S2: Interrupt circuit A, I/O area P
- S3: I/O address 0
- S4: Sensor signals symmetrical
- S5: Sensor signals +5 V (channel 1)
- S6: Sensor signals + 5 V (channel 2)

Blocks

For the programming example, the data block DB 168 "P_data" is used. It has the same format as the corresponding standard data block. The data necessary for the example has also been entered.

The following blocks are used:

Block	Name	Purpose
OB 1	Cycle	Cyclic program scanning
OB 40	Interrupt	Interrupt processing
OB 100	Start-up	Cold restart processing
DB 170	P_data	Data block for positioning
FC 169	STRU_WEG	Structure block
FC 170	STEU_WEG	Control block

Addresses

The inputs and outputs are mapped onto memory bits at the beginning and end of OB 1. Within the test program, only the memory bits are used.

Addresses

The inputs and outputs are mapped onto memory bits at the beginning and end of OB 1. Within the test program, only the memory bits are used.

Signal	Memory Bit	Description
I 2.0	M 180.0	Execute function
I 2.1	M 180.1	Write zero displacement
I 2.2	M 180.2	Disable/enable interrupts
I 2.3	M 180.3	Delete interrupt display
I 2.4	–	Unassigned
I 2.5	–	Unassigned
I 2.6	–	Unassigned
I 2.7	–	Unassigned

Signal	Memory Bit	Description
Q 2.0	M 181.0	Execute function
Q 2.1	M 181.1	–
Q 2.2	M 181.2	Interrupts have been enabled
Q 2.3	M 181.3	Interrupt display
Q 2.4	–	Unassigned
Q 2.5	–	Unassigned
Q 2.6	–	Unassigned
Q 2.7	M 181.7	Error has occurred

The following memory areas are also occupied:

Bit Memory Address Area	Description
MB 182	Edge memory bit
MB 182	Error memory bit
MB 184 bis MB 189	Error bytes of the PAFE parameter

Start-up Program and Error Responses

Start-up Program

The start-up program is in OB 100. When OB 100 has been processed, you can check the following entries with “Monitor/Modify variable”:

- DB 170.DBB 2 to DBB 7: Product code of the module
- DB 170.DBB 8 to DBB 13: Firmware version
- DB 170.DBB 14 and DBB 15: Hardware version
- DB 170.DBB 46: B#16#041 (“Positioning” mode)
- DB 170.DBW 48: Data block number
- DB 170.DBW 52: Basic address of the module

The actual value

- DB 170.DBD 60: Actual value (BCD-coded or binary-coded, depending on how the BCD parameter is assigned)

  is the value of the zero displacement.
- The returned position number

  DB 168.DBW 56 Number of position to be approached

  is the value W#16#00FF (no position selected).

If all inputs show the signal state ‘0’, no output may be activated.

Responses to Errors

If an error or fault occurs during execution of the start-up program, the cyclic block calls are no longer processed; the error memory bit is set.

After every block call in the cyclic program, an error is flagged when an error occurs (BR = ‘0’), which in turn causes a group error message to be output at Q 1.7 (M 191.7).

In the case of a group error message, the associated error bit indicates which block call has caused the error. A precise description of the error can be found in the corresponding PAFE byte and in the error words of the data block (see the IP 240 Manual, Sections 10.23.1 “Configuring Function Block” and 10.23.2 “Control Function Block”).

Cyclic Program

General Remarks

The cyclic program is in OB 1.

At the beginning of the program, the inputs are mapped to memory bits which are then used in the rest of the program. At the end of the program, the control memory bits are transferred to the outputs and displayed.

Reading the Actual Value, End Value, Position Number and Status Bits

The FC 168 function is called absolutely with function B#(1,0); this means that it is **always** processed and reads the actual value, the end value, the position number and the status bits in every program cycle.

Specifying a Function

The example is structured such that by activating the input I 1.0 (M 190.0), you can transfer any function to the module.

Proceed as follows:

1. Enter, for example with “Monitor/Modify variable”, the appropriate data in the data block (see below).
2. Specify the desired function in the data word DBW 38.
3. Transfer the function by briefly activating the input I 1.0.

In the event of an error, the group error message Q 1.7 is set. If, for example, values with an invalid range are transferred, the module returns a corresponding error in the data word DBW 20 (MB 196 then shows B#16#01).

Synchronization

Before any positioning can occur, the recording of the actual value must be synchronized. We use software synchronization.

Through transfer of the corresponding control bits

- DB 168.DBX 72.5 SOSY = TRUE,
- DB 168.DBW 38 FUNCTION = B#(20,0)

with the input I 1.0 (M 190.0), the actual value is set to the value of the last transferred zero displacement.

The control bit SOSY should be reset so that synchronization is not repeated the next time the control bits are transferred.

Specifying a Position

With the control word

- DB 168.DBW 38 FUNCTION = B#(21,1)

and brief activation of the input I 1.0 (M190.0), position 1 is specified for approaching.

The status bits now show the traversing direction to the position as well as the reaching of the clearance values:

- DB 168.DBX 59.1 RICH,
- DB 168.DBX 59.2 BEE1,
- DB 168.DBX 59.3 BEE2,
- DB 168.DBX 59.4 BEE3,
- DB 168.DBW 56 W#16#0001 (returned position number).

With the control word

- DB 168.DBW 38 FUNCTION = B#(21,2)

and brief activation of the input I 1.0 (M190.0), position 2 is specified for approaching. The positioning process for position 2 is as described above.

Writing Zero Displacement

With the input I 1.1 (M 190.1), you can transfer a new zero displacement to the module. You must write the desired value to the data block beforehand:

- DB 168.DBD 92 Zero displacement

The zero displacement is added to the current actual value.

Writing Clearance Values

The clearance values around a position can be modified during cyclic operation.

- DB 168.DBD 100 BEE1,
- DB 168.DBD 104 BEE2,
- DB 168.DBD 108 BEE3,
- DB 168.DBW 38 FUNCTION = B#(6,0).

With brief activation of the input I 1.0 (M190.0), the new clearance values are taken over by the module.

Setting Digital Outputs

The LEDs in the front panel allow you to observe the setting of the digital outputs D1 and D2 on the module.

With the DAV parameter of FC 167, you define the behavior of the digital outputs of the module at start-up (for example, DAV = 0; outputs control the traversing speed with separate activation according to D1 = rapid speed and D2 = creep speed). You define the release of the digital outputs with the control bits:

- DB 168.DBX 72.0 FREE = TRUE,
- DB 168.DBX 72.1 MANUAL = FALSE,
- DB 168.DBW 38 FUNCTION = B#(20,0).

With brief activation of the input I 1.0 (M 190.0), the control bits are transferred to the module and become effective immediately. The digital outputs are set for the duration of the positioning process.

With the control word

- DB 168.DBW 38 FUNCTION = B#(20,1)

and by activating the input I 1.0 (M 190.0), the digital outputs are reset regardless of the positioning process.

Interrupt Program

Interrupt Block

The interrupt program is located in the organization block OB 40.

Enabling Interrupts

In the start-up program, the module is structured such that when the clearance value BEE1 is reached (PRA1 = W#16#0001) an interrupt is generated. Interrupt generation is initially blocked (control bit AMSK = ‘1’).

In the cyclic program, a positive edge at input I 1.2 (M 190.2) causes the control bit AMSK to be reset and transferred to the module (FC 168 with function B#(20,0). Now an interrupt is generated when the clearance value BEE1 is reached. The enable of interrupt generation is signalled at output Q 1.2 (M 191.2).

The interrupt enable is canceled through transfer of the control bit AMSK to the module with negative edge at input I 1.2 (M 190.2).

Acknowledging Interrupts

In the interrupt program, the FC 168 function is called by means of function 3,0 (read interrupt request bytes). The interrupt request bytes are transferred from the module to the data block. These contain the cause of the interrupt (for example, interrupt generation when the clearance value BEE1 is reached: DB 168.DBX 41.2 is set). When an interrupt is generated in this way, the memory bit M 191.3 is set, which then causes the interrupt to be signalled via output Q 1.3 in the cyclic program.

In the cyclic program you can delete the interrupt display again with positive edge at input I 1.3 (M 191.3).

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Q

R

S

Z

2 Module Description and Accessories

2.1 General Technical Specifications

Climatic Environmental Conditions	
Temperature	
Operation	0 to +55 °C (Intake air temperature, measured at the bottom of the module)
Storage/shipping	- 25 to + 70 °C
Temperature change	
- Operation	10 °C/h max.
- Storage/shipping	20 °C/h max.
Relative humidity	to DIN 40040 15 to 95% (indoors) noncondensing
Atmospheric pressure	
- Operation	860 to 1060 hPa
- Storage/shipping	660 to 1060 hPa

Electromagnetic Compatibility (EMC) Noise Immunity	
Damped oscillatory wave test (1 MHz)	to IEC 255-4
Digital-inputs and outputs	1 kV
Static electricity	to IEC 801-2 (discharge on all parts accessible to the user during normal operation)
Test voltage	2 kV
Radiated electro-magnetic field test	to IEC 801-3 Test field strength 3 V/m
Fast-transient burst test	to IEC 801-4
Digital-inputs and outputs	1 kV

Mechanical Environmental Conditions	
Vibration	to IEC 68-2-6
- Tested with	10 to 57 Hz, (constant amplitude 0,15 mm)
	57 to 150 Hz, (constant acceleration 2 g)
Shock	IEC 68-2-27
-Tested with	12 shocks (semisinusiodal 15 g/11 ms)
Free Fall	IEC 68-2-32
- Tested with	Height of fall 1 m

Specifications on IEC/VDE safety	
Degree of protection	to IEC 529
- Implementation	IP 20
- Class	I to IEC 536
Insulation rating for the digital outputs	to VDE 0160
- Nominal insulation voltalge between electrically independent circuits **and** circuits connected to central ground	30 V DC
Test voltage at a rate voltage U_e of the AC or DC circuit of U_e=0 to 50 V	sinusoidal, 50 Hz 500 V

2.2 Technical Specifications

The IP 240 has two independent channels.

In the **IP 252 expansion** mode, the encoder signals are acquired as in the position decoding and positioning modes. The data relating to pulse inputs for position decoding therefore also apply to the **IP 252 expansion**.

Current consumption, internal	Max. 0.8 A at 5 V without encoder supply
Weight	Approx. 450 g
Width of the module	1 SPS=20 mm

2.2.1 Position Decoding and Positioning

Pulse inputs	
Encoders	Incremental encoders with the following characteristics:
- Encoder signals	Two pulse trains displaced by 90° (Channels A and B), one reference signal (Channel Z) The Z signal is evaluated in zero mark monitoring and reference point approach during signal state A="1" and B="1". For the duration of signal Z, states A="1" and B="1" may only occur once (Section 13.1.1).
- Encoder output circuits	with **symmetrical pulse train** to RS 422 A or similar, rated encoder voltage 5 V, connection to inputs: A and $\overline{A}$, B and $\overline{B}$, Z and $\overline{Z}$
	with **asymmetrical pulse train**, e.g. push-pull, open collector (external pull-up resistors required) , rated encoder voltage 24 V, connection to inputs: A*, B*, Z*
Binary input	
Encoders	e.g. BERO proximity switches
- Encoder output circuit	Switching to P potential Operating voltage 24 V, connection to input: IN (preliminary contact)

Input frequencies

Pulse inputs:		
- Symmetrical signals	max. 500 kHz	in position decoding and positioning mode
	max. 200 kHz	in IP 252 expansion mode
- Asymmetrical signals	max. 25 kHz	for 100 m cable [1]
	max. 100 kHz	for 25 m cable [1]
Binary input:	max. 100 Hz	

2.2.2 Counting

Pulse input

Encoders	e.g. incremental encoders
- Encoder output circuit	Switching to P potential, encoder voltage rating 24 V, connection to input: CLK (clock)

Binary input

Encoders	e.g. BERO proximity switches
- Encoder output circuit	Switching to P potential, operating voltage 24 V, connection to input: GT (gate)

Input frequencies

Pulse input:	max. 25 kHz	for 100 m cable [1]
	max. 100 kHz	for 25 m cable [1]
Binary input:	max. 100 Hz	

[1] Max. encoder output resistance 1 k
Max. capacitance per unit length 100 pF/m

2.2.3 Inputs/Outputs

The IP 240 provides two options for connecting sensors to the pulse inputs:
- All sensor signals can be routed to the 15-pin subminiature D socket connectors X2/X4 (Section 4.2.2)
- Clock signals up to 10 kHz can also be routed over the 7-pin plug connectors X3/X5 (Section 4.2.2).

The sensor power supply is only available at the 15-pin subminiature D socket connectors.

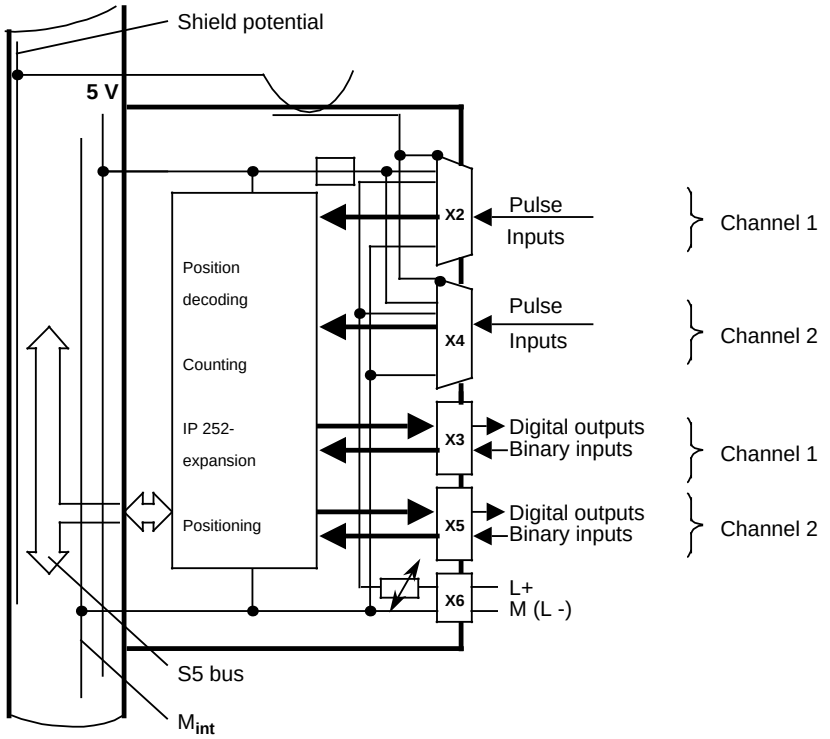


Fig. 2-1. Front Connectors

Warning

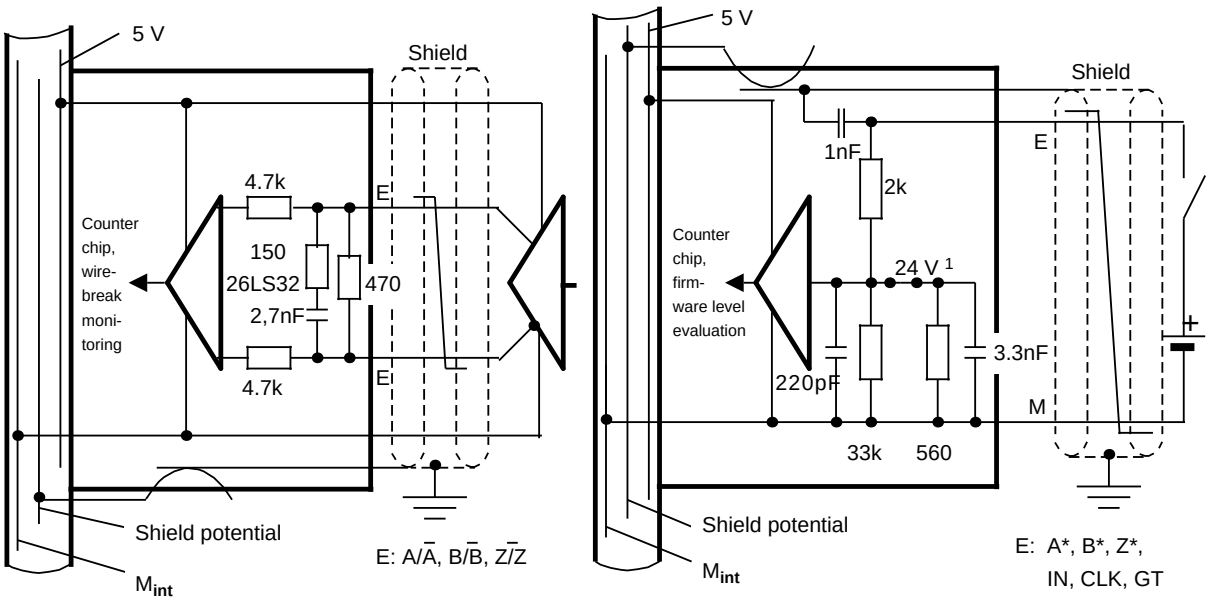
To ensure noise immunity, all inputs, outputs and the 24 V supply on the IP 240 must be connected using shielded, twisted-pair cables.

Terminal M (L-) is connected on the IP 240 to the module ground (M_{int}).

Inputs

Terminals	**A and $\overline{A}$ B and $\overline{B}$ Z and $\overline{Z}$**	**A* B* Z***	**IN (prelim. contact) CLK (CLOCK) GT (GATE)**
Encoder signals	Symmetrical (RS 422 A)	Asymmetrical	
Rated voltage	5 V	24 V	24 V
Galvanic isolation	no	no	no

Data for rated voltage	**5 V** symmetrical pulse train	**24 V**
Input voltage ranges	to RS 422 A	
”0”-Signal		- 30to+ 5.0 V
”1”-Signal		+16 to+ 30 V
Input currents	to RS 422 A	
”0” signal		- 16to+ 1.9 mA
”1” signal		+ 6 to+ 13 mA
”1” signal typ.		8.5 mA
Edge steepness of the input signals	min. 5 V/µs	min. 10 mV/µs
Perm. quiescent current for ”0” signal		max. 1.5 mA
Delay time of the input circuit		0.8 to 4 µs
Input resistance		2.6 k
Length of shielded and twisted-pair cable	max. 30 m (100 ft)	max. 100 m (325 ft)
Input circuit	Fig. 2-2a.	Fig. 2-2b.



1 Inputs A*, B*, Z*, IN, CLK and GT must be set to 24 V level on coding switches S5 and S6 (Section 5.3.2).

a) Encoders to RS 422 A (symmetrical pulse train) *b) 24 V encoder*

Fig. 2-2. Block Diagram of the Input Circuit for Encoders to RS 422 A

Digital outputs

Number of outputs	4 (2 per channel)
Galvanic isolation	yes
in groups of	1
Supply voltage Vp	
Rating	24 V DC
Ripple	3.6 V max.
Permissible range (including ripple)	20 to 30 V
Output current for ”1” signal	0.5 A max.
Short-circuit protection	Fuse, 0.8 A fast
Voltage induced on circuit interruption limited to	- 23 V
Switching frequency	
resistive load (24 V/50 mA)	200 Hz max.
(max. 8,5 W)	2 Hz max.
inductive load (time constant max. 50 ms)	
lamp load (max. 5 W)	8 Hz max.
Simultaneity factor at 55 °C (Number of outputs simultaneously energized)	100 %
Residual current at ”0” signal	1 mA max.
Output voltage at ”1” signal	Vp - 3 V min.
Max. length of	
shielded twisted-pair cable	1000 m (3300 ft)
Rated insulation voltage to VDE 0160	30 V DC
Insulation group	C
tested at	500 V AC

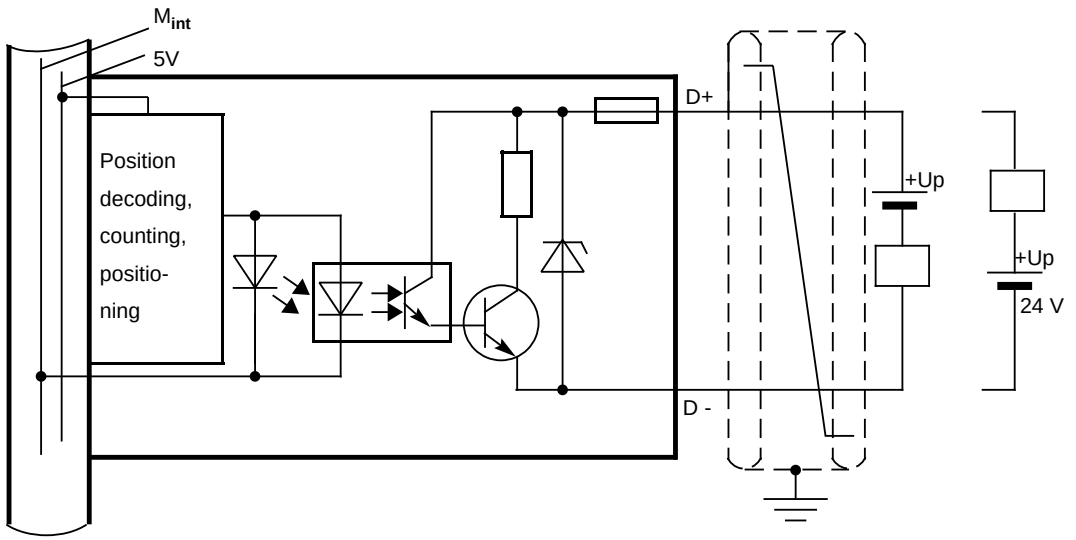


Fig. 2-3. Block Diagram of the Output Circuit

Encoder supply
The power supply for 5 V encoders taken from the programmable controller's power supply and made available over subminiature D socket connectors X2 and X4 (pins 4 and 10) (Section 4.2.2).
If 24 V is needed, the IP 240 must be powered via the external connection on connector X6 provided for this purpose (24 V, 0 V). The 24 V input is connected internally with encoder supply outputs on subminiature D socket connectors X2 and X4 (pin 2) (Section 4.2.2). The external supply voltage is not filtered on the module.

Encoder supply

• 5 V DC	4.75 V to 5.25 V max. 0.8 A total
Short-circuit protection	Fuse 1.6 A T
• 24 V DC	20 V to 30 V max. 0.6 A total
Overload protection	PTC thermistor I_{rated} = 0.7 A

Influence of cable length on the encoder supply voltage
If the encoder voltage is provided by the IP 240, the voltage level and the total voltage line cross-section must be such that the voltage on the encoder lies within the stipulated tolerance.
If the supply voltage is not sufficient to supply 5 V DC for the encoder, the encoder must be provided with power from another source. The required voltage can be fed in over the 24 V (L+)/M terminal on connector X6. Note that, when supplying incremental encoders with symmetrical outputs (to RS 422A) from another source, the difference in the earth potential between the encoder and the module electronics may be no more than ±5 V.

2.3 LEDs

LEDs display the following information:
- Hardware faults on the module (**M**odule **F**ault = **MF**),
- The states of the digital outputs (**D1** and **D2**),
- Wirebreaks and short-circuits in the encoders with symmetrical pulse trains (**W**ire-**B**reak=**WB**).

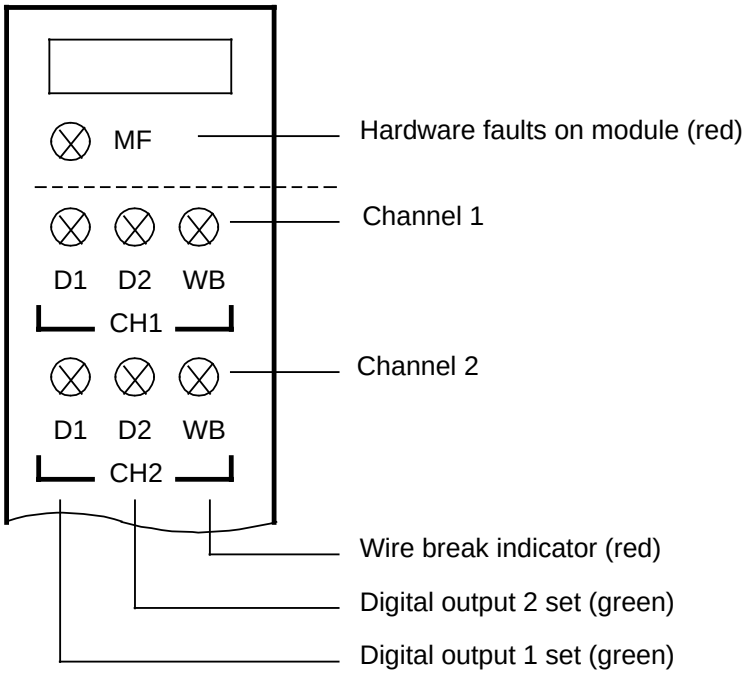


Fig. 2-4. LEDs

2.4 Order Numbers

		Order No.
Module without instruction manual		**6ES5 240-1AA12**
Adapter casing for 2 modules in S5-115U		**6ES5 491-0LB12**
Manual	English	**6ES5 998-0TB22**
”	German	**6ES5 998-0TB12**
”	French	**6ES5 998-0TB32**
”	Italian	**6ES5 998-0TB52**

Function blocks

Position decoding, counting and IP 252 expansion mode

For the S5-DOS operating system	**6ES5 848-8JB02**
For the MS-DOS/S5-DOS/MT operating system	**6ES5 848-7JB02**

Positioning mode

For the S5-DOS operating system	**6ES5 848-8JC02**
For the MS-DOS/S5-DOS/MT operating systems	**6ES5 848-7JC02**

Fuse 0.8A F e. g. Wickmann No.TR5F 19370K
1.6A T Wickmann No.TR5T 19372K

Position encoders with symmetrical signals
e. g. Siemens, No. 6FC9320-...

Connecting cables for 6FC9320-3..00 position decoders

5m	**6ES5 705-3BF01**
10m	**6ES5 705-3CB01**
20m	**6ES5 705-3CC01**
32m	**6ES5 705-3CD21**

Connectors Socket connector, 2-pin (Weidmüller, BLA 12817.0)
Socket connector, 7-pin (Weidmüller, BLA 12822.0)

3 Addressing

The IP 240 module reserves an address space of 16 bytes in the I/O areas. All data are exchanged via these areas, which can be read out and written to by the S5 CPU. The data transfer is handled by a standard function block. It is merely necessary to set the desired starting address and the I/O area (P or Q area) via coding switches on switchbanks S2 and S3 on the module.
For address decoding, the IP 240 needs the memory-I/O select signal PESP in addition to the S5 bus addresses A 0 to A 11.

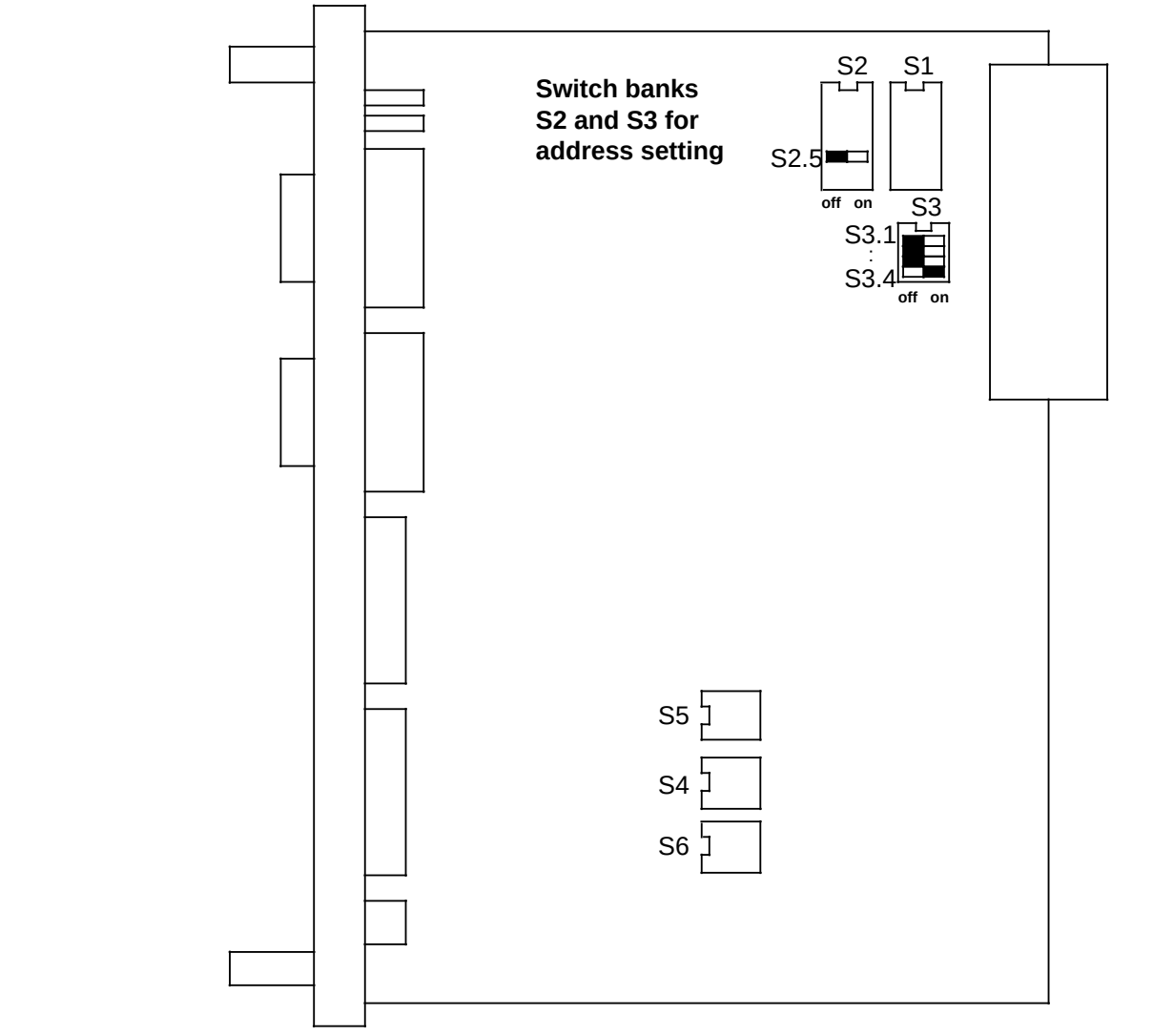
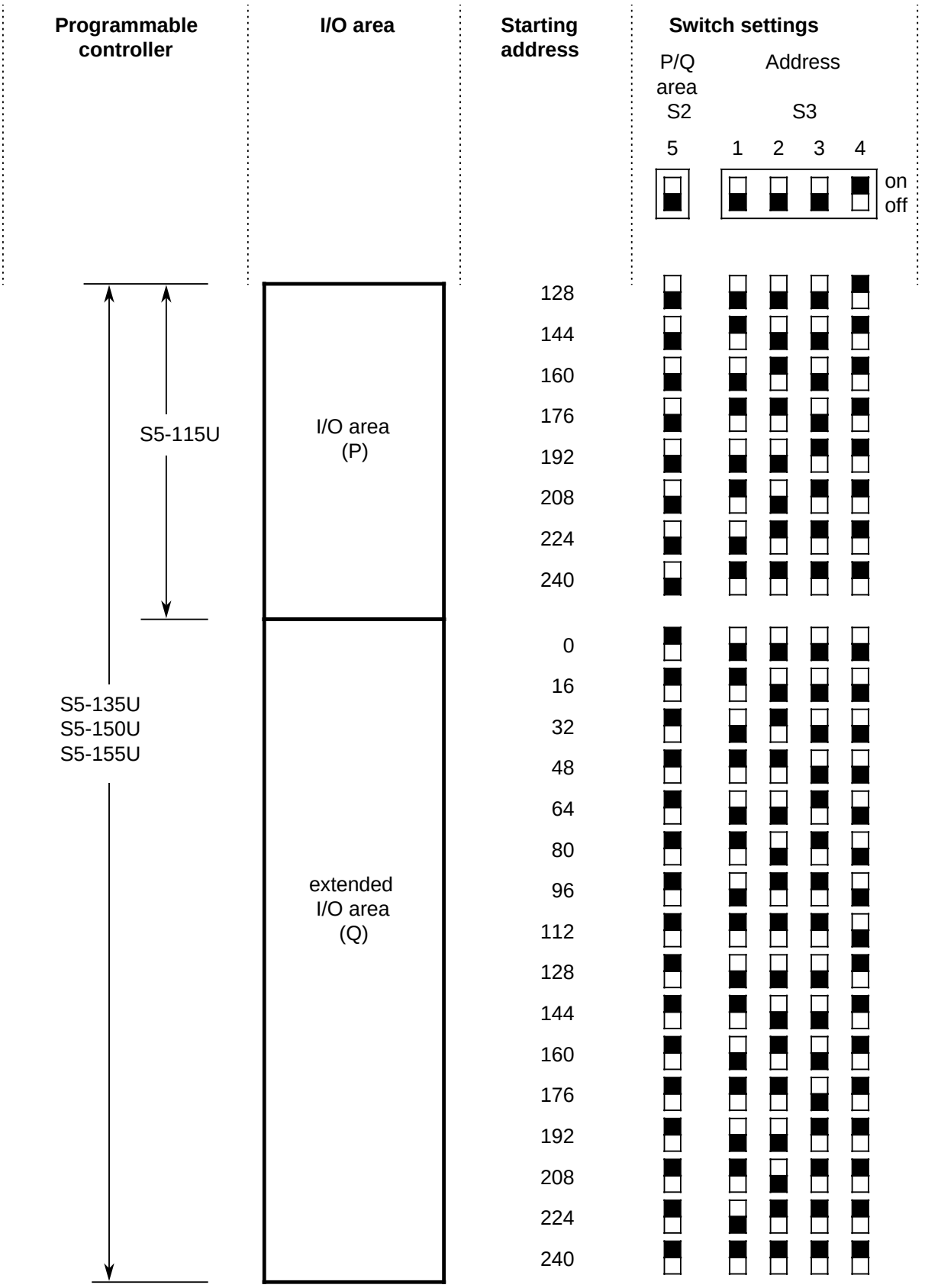


Fig. 3-1. Locations of the Address Switches

Note

The modules are delivered with a set starting address of 128 in the normal (P) I/O area. Before start-up, make sure that no two modules reserve the same


Programmable controller
I/O area
Starting address
Switch settings
P/Q area S2
Address S3
5
1 2 3 4
on
off
S5-115U
S5-135U
S5-150U
S5-155U
I/O area (P)
extended I/O area (Q)
128
144
160
176
192
208
224
240
0
16
32
48
64
80
96
112
128
144
160
176
192
208
224
240

Use of the IP 240 in expansion units S5-183U, S5-184U, S5-185U and S5-186U
If you use the IP 240 in one of these EUs, set the start address on switchbank S3 as explained above.

Setting the I/O area or the extended I/O area:

- S5-183U and S5-184U expansion units
  - Set the I/O area or the extended I/O area on the interface module.
  - Always put switch 2.5 on the IP in the ”off” position.

- S5-185U and S5-186U expansion units
  - Set I/O area or extended I/O area on the interface module.
  - Set I/O area or extended I/O area on the IP.

Note:
The module address must lie in the P area if the IP 240 is to generate process interrupts over I/O byte PY0.

5 Operation

Before startup you must set various coding switches on the module.
You can stipulate

- interrupt generation with switchbanks S1 and S2 (Section 5.1)
- disabling of the digital outputs with switchbank S4 (Section 5.2)
- encoder signal matching with switchbanks S5 and S6 (Section 5.3)

The locations of the switchbanks and the fuses are shown in Fig. 5-1. The switch settings in the figure are factory setttings.

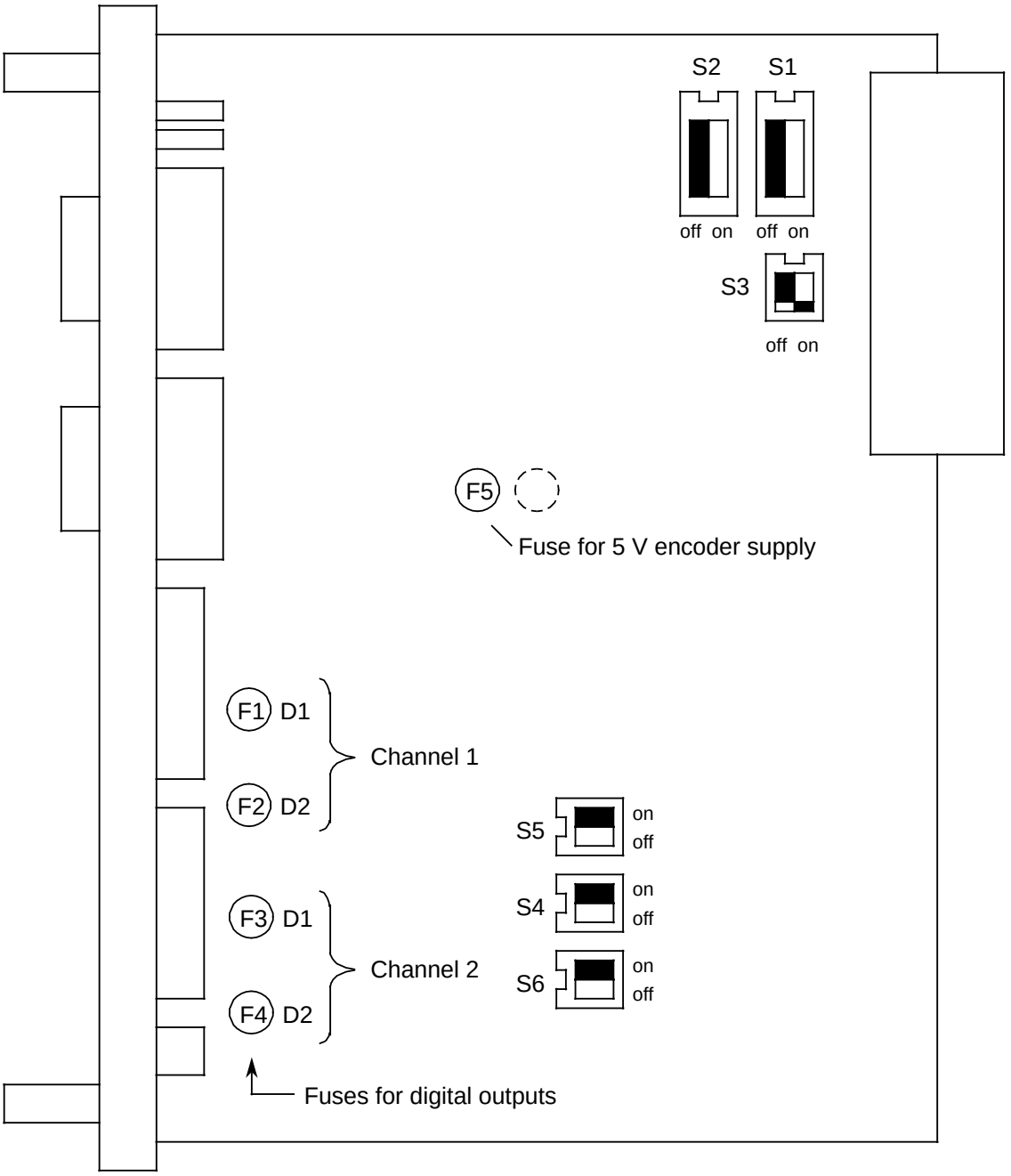


Fig. 5-1. Locations of Switchbanks and Fuses

5.1 Settings for Interrupt Generation

The processing of interrupt signals makes it possible to respond rapidly to status changes.
In the SIMATIC S5 programmable controllers, a distinction is made between two types of interrupts:

- "Servicing IRx interrupt circuits" (S5-115U, S5-135U and S5-155U in the 155U mode)
- "Reading I/O byte 0" (S5-150U and S5-155U in the 150U mode).

5.1.1 IRx Interrupt Circuits

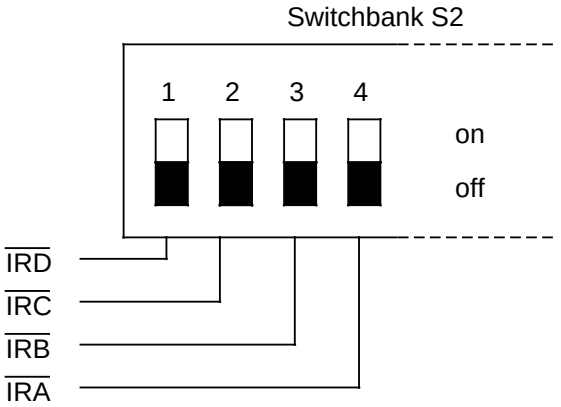
The interrupt signal generated on the IP 240 can be routed to the S5-CPU via one of four interrupt circuits $\overline{IRA}$ to $\overline{IRD}$ for interrupt processing. The following must be taken into account:

- the possible slots on the IP 240 (4.1.2)
- the capabilities of the programmable controllers and individual CPUs (Table 5-1)
- the required switch settings on the IP 240

Table 5-1. Allocation of Serviceable Interrupt Circuits

PLC	CPU	CPU slot	Serviceable interrupt circuit
S5-115U	941		$\overline{IRA}$, $\overline{IRB}$
	942, 943, 944		IRA, IRB, IRC, IRD
S5-135U	922 or 928	11	$\overline{IRA}$
	922 or 928	19	$\overline{IRB}$
	922 or 928	27	$\overline{IRC}$
	922 or 928	35	IRD
S5-155U (155U mode)	946/947, 922 or 928	11	$\overline{IRA}$
	946/947, 922 or 928	51	$\overline{IRB}$
	922 or 928	91	$\overline{IRC}$
	922 or 928	99	IRD

Allocation of coding switches on switchbank S2 to the IRx interrupt circuits
Use coding switches S2.1 to S2.4 to set the IRx interrupt circuit to be used.



Coding switches S2.1 to S2.4
on : the corresponding interrupt circuit is used
off: the corresponding interrupt circuit is not used

Fig. 5-2. Allocation of Coding Switches on Switchbank S2 to the IRx Interrupt Circuits

If several IP 240 modules use one interrupt circuit, the current interrupt source must be determined by reading the interrupt request bytes of all modules or by additonally evaluating I/O byte 0. This must be taken into account in the STEP 5 program due to the system characteristics of the S5-115U CPUs (Section 5.1.2).

Note

- In the S5-115U, S5-135U and S5-155U, only one of the coding switches S2.1 to S2.4 may be closed at any given time. In the S5-150U, these switches must always be set to ”off”.
- If the 6ES5 434-7LA11 digital input module is used in the S5-115U, interrupt circuit IRA is already reserved and is no longer available for IP 240 modules.
- In the S5-135U, interrupt-driven program processing must be level-triggered (this corresponds to the basic settings in DX 0).
- In the S5-155U (155U mode), the selected interrupt circuit must be set on the CPU 946 and enabled additionally in DX 0.

5.1.2 I/O Byte 0 (PY)

In the S5-150U and S5-155U programmable controllers (in the 150 U mode), an interrupt request from up to eight modules is detected by reading I/O byte 0. Evaluation of I/O byte 0 in IP 240 modules is possible only when theses modules are addressed in the P area.

For interrupt generation over an IRx interrupt circuit, the **additional** evaluation of I/O byte 0 enables the use of one interrupt circuit for several IP 240s.

Interrupt generation with I/O byte 0
Each bit in I/O byte 0 can be reserved by **one** module with interrupt capablity. Switches S1.1 to S1.8 on switchbank S1 are available on the IP 240 for this purpose. By defining which bit is to be set for an interrupt signal on the module, the priority can be determined with which the interrupt request is processed if two or more interrupt requests are pending simultaneously. Bit 0.0 has the highest priority and bit 0.7 the lowest.

The module with the highest priority (I/O byte 0.0) is declared to be the master module of the programmable controller. It is used to mask all unassigned bits of I/O byte 0. If an IP 240 is used as the master module, switch S1.1 must be closed (”on” position). Only one other switch on switchbank S1 may be set to ”on” to mask the unassigned bits in the I/O byte 0. If several bits in I/O byte 0 are unassigned, the interrupt OBs for the non-masked bits may not be programmed.

On the remaining IP 240 modules, designated as slaves, the switch for the corresponding bit in I/O byte 0 and switch S2.7 must be closed ("on" setting). All other switches on bank S1 must be set to the ”off” position.

Switch S2.8 must be closed on both master and slave modules to enable interrupt generation via the I/O byte 0. Only then does the IP 240 make data available when the S5 CPU reads I/O byte 0.

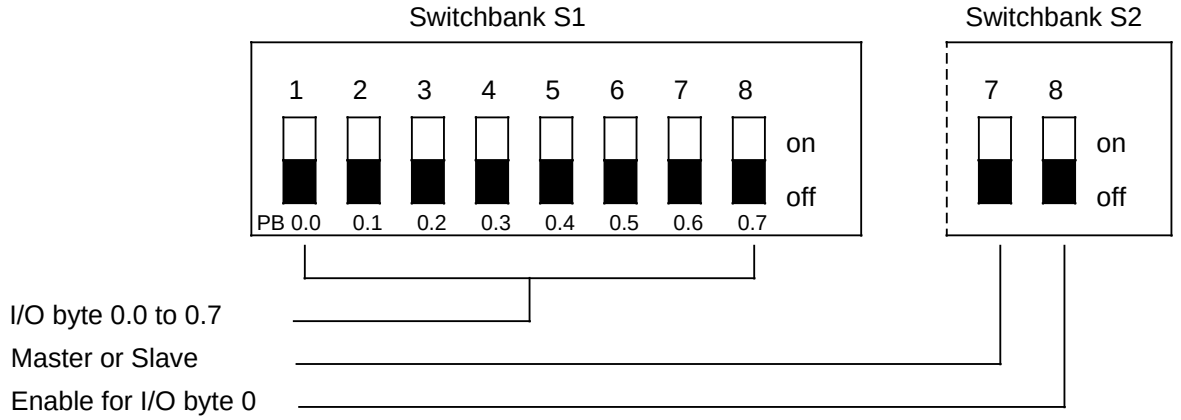


Fig. 5-3. Allocation of Coding Switches on Switchbanks S1 and S2 to Interrupt Generation with I/O Byte 0

The coding switches on banks S1 and S2 shown in Fig. 5.3 have the following meaning:

on: The corresponding bit of I/O byte 0 is set in response to an interrupt signal on the I/O module. And on a master module: the corresponding bit of I/O byte 0 is not reserved by a slave module.

on: The I/O module is operated as slave
off: The I/O module is operated as master

on: Enabling of interrupt generation over I/O byte 0

Warning

No input module may be set to address IB 0 when I/O byte 0 is enabled with switch S2.8.
In additon to switch S1.1, only one other switch (S1.2 to S1.8) may be closed on switchbank S1.
In the S5-155U, process interrupt generation via I/O byte 0 must also be enabled in DX 0.

Calling the interrupt OBs in the S5-150U and S5-155U (150 mode)
In the S5-150U and S5-155U (150 mode), a change in one of the bits in I/O byte 0 invokes the corresponding interrupt OB at the next block boundary. When you initialize the module with function blocks 167, 169, and 171 (Sections 10.23.2 and 8.3.1), you can set the ABIT parameter to specify whether the interrupt OB is to be invoked after every signal change or only when the bit goes from 0 to1.

ABIT parameter:

ABIT : KY x,y

- x>0 : The interrupt OB is invoked on every signal change.
- x=0, y=0 to 7 : The interrupt OB is invoked only on a signal change from 0 to 1. Y is the number of the bit in I/O byte 0 which you have set on switchbank S1.

Example for setting the coding switches
Three IP 240s are to be enabled for interrupt generation. One IP 240 is to be operated as master module and the other two as slave 1 and slave 2. Slave 1 is assigned to PY 0.1 and slave 2 to PY 0.2. Bits PY 0.3 to PY 0.6 are reserved by other modules. PY 0.7 is not used and must be masked on the master module or else OB9 must not be programmed.

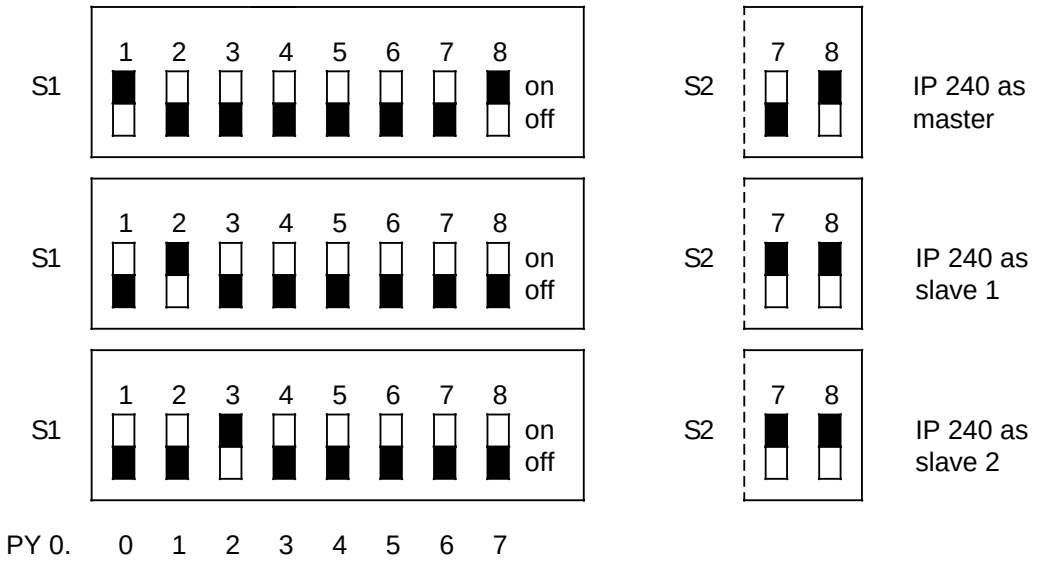


Fig. 5-4. Settings of the Coding Switches (Example)

If slave 1 and slave 2 generate a process interrupt, the value 06_H is stored in PY 0.

Additional evaluation of I/O byte 0 for interrupt generation over the IRx interrupt circuit (S5-115U, S5-135U and S5-155U (155 mode))
I/O byte 0 on the IP 240 can also be scanned when the interrupt is generated over interrupt circuit IRx. Additonal evaluation of I/O byte 0 makes it possible to operate several IP 240s on a single interrupt circuit. When this option is used, however, I/O byte 0 may not be reserved by any other module.

Required switch settings on the IP 240:
- Use the coding switches on bank S1 to determine which bit in I/O byte 0 is to be reserved. (Switch S1.1 corresponds to bit 0.0 etc.)
- Close switches S2.7 and S2.8 (”on” position)

After reading I/O byte 0, only those bits reserved by the IPs must be evaluated.

Additional programming in the organization blocks for the S5-115U:

a) The interrupt service routine must be programmed in an FB so that it may execute several times.
   - I/O byte 0 must be read once at the beginning of interrupt processing to determine which IP triggered the interrupt.
   - I/O byte 0 must also be read at the end of the interrupt service routine. If a new interrupt request is pending, it must be serviced without exiting the interrupt OB.

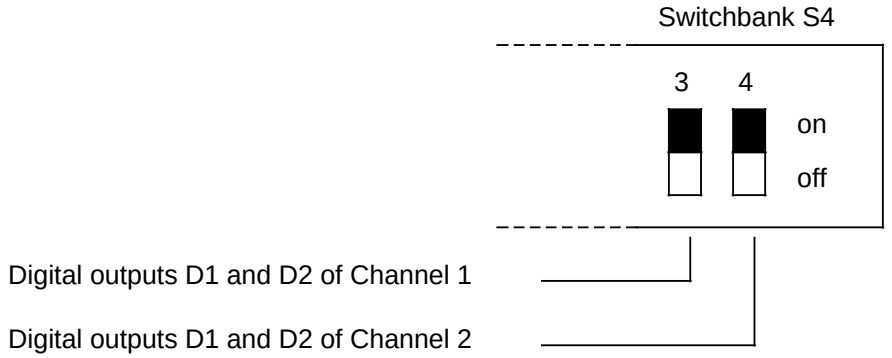
Note:
Failure to include these steps in the STEP 5 program will block all further interrupt generation on this circuit should a single interrupt fail to be serviced.

b) So that the CPU does not go to the stop state with a time-out, the following sequence of statements must be inserted into OB21 and OB22.

STL OB 21 and OB 22	STL FBn	Explanation
JU FBn NAME: XYZ ... BE	L RS 16 L KH FEFF AW T RS 16 BE	This sequence of instructions prevents updating of word 0 in the process input image.

5.2 Output Inhibit (BASP)

If the S5 CPU goes to the stop mode, this does not affect the IP 240 firmware; the module continues to run in the specified mode and can also activate the digital outputs when the programmable controller is at stop. However, all digital outputs on the IP 240 can be deenergized with an output inhibit (BASP) signal generated by the S5 CPU in the STARTUP and STOP states.
The behaviour of the outputs when an output inhibit is applied can be selected via switches 3 and 4 on bank S4 to suit the process. When the BASP signal is revoked, the outputs assume the state stipulated by the IP 240.



on: Output inhibit (BASP) switches the digital outputs to the inactive state
off: Output inhibit (BASP) does not affect the states of the outputs

Fig. 5-5. Setting the Command Output Inhibit "BASP" on Switchbank S4

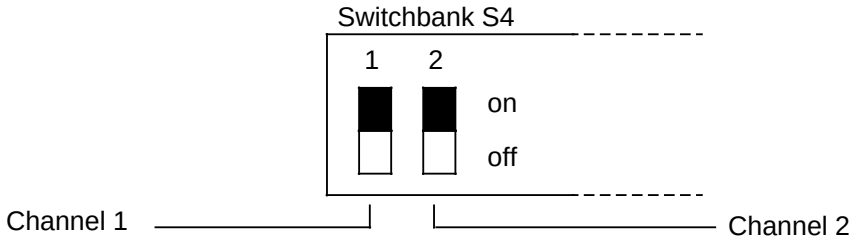
5.3 Matching to Encoder Signals

Encoders with 24 V DC signals and encoders which generate signals to the RS 422 A or a similar standard can be connected to the inputs of the IP 240. The user can set coding switches for matching the IP 240 to the encoder signals.

5.3.1 Settings for Symmetrical or Asymmetrical Signals

All incremental encoders whose outputs comply with the RS 422 A standard supply symmetrical signals A, B and Z and their inverted signals. These encoders have line drivers at the outputs, e.g. 26LS31, 75172 or 75174.

All incremental encoders whose outputs produce a 24 V DC level supply asymmetrical signals A*, B* and Z*. These encoders have stages which switch to P potential at the outputs or open collector outputs connected to 24 V via external pull-up resistors.



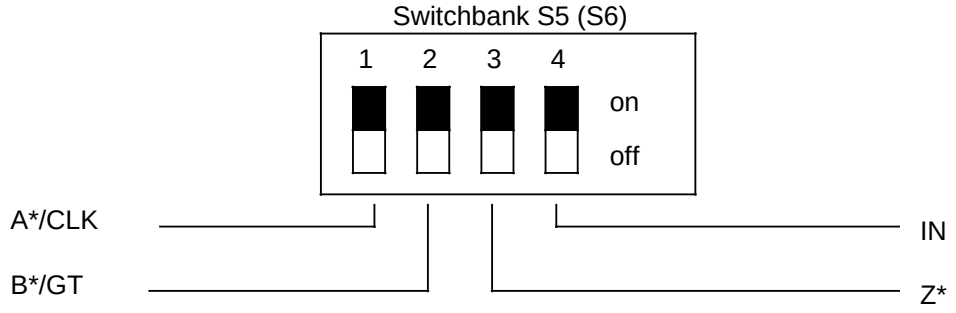
On: Asymmetrical signals A*, B*, Z*
Off: Symmetrical signals A/ $\overline{A}$, B/$\overline{B}$, Z/$\overline{Z}$

Fig. 3-6. Setting Switchbank S4 for Symmetrical or Asymmetrical Signals

5.3.2 Settings for Encoder Signal Levels

Input signals A*/CLK, B*/GT, Z* and IN must be set to 24 V DC on switchbank S5 for channel 1 and on switchbank S6 for channel 2.

> **Warning**
>
> A 5 V DC level setting is not permissible at the present time for reasons of noise immunity. All switches on the switchbank must be set to ”on”.



On: 24 V DC input level
Off: not permissible

Fig. 5-7. Setting the Encoder Signal Level on Switchbanks S5 and S6

Siemens AG
AUT E 148
Postfach 1963

D-92209 Amberg
Federal Republic of Germany

From:

Your Name: _____

Your Title: _____

Company Name: _____

Street: _____

City, Zip Code: _____

Country: _____

Phone: _____

Please check any industry that applies to you:

- ☐ Automotive
- ☐ Chemical
- ☐ Electrical Machinery
- ☐ Food
- ☐ Instrument and Control
- ☐ Nonelectrical Machinery
- ☐ Petrochemical
- ☐ Pharmaceutical
- ☐ Plastic
- ☐ Pulp and Paper
- ☐ Textiles
- ☐ Transportation
- ☐ Other _____

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